

FIG. 1

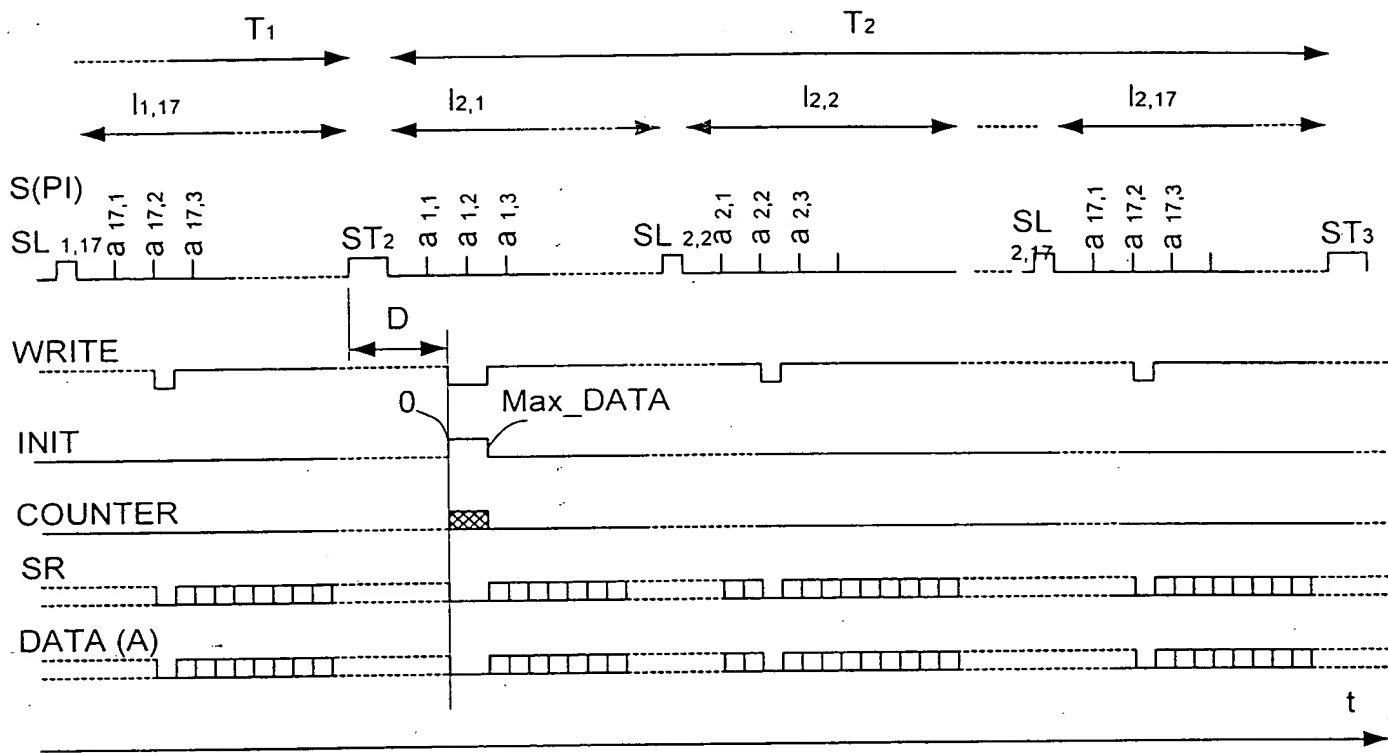


FIG. 2

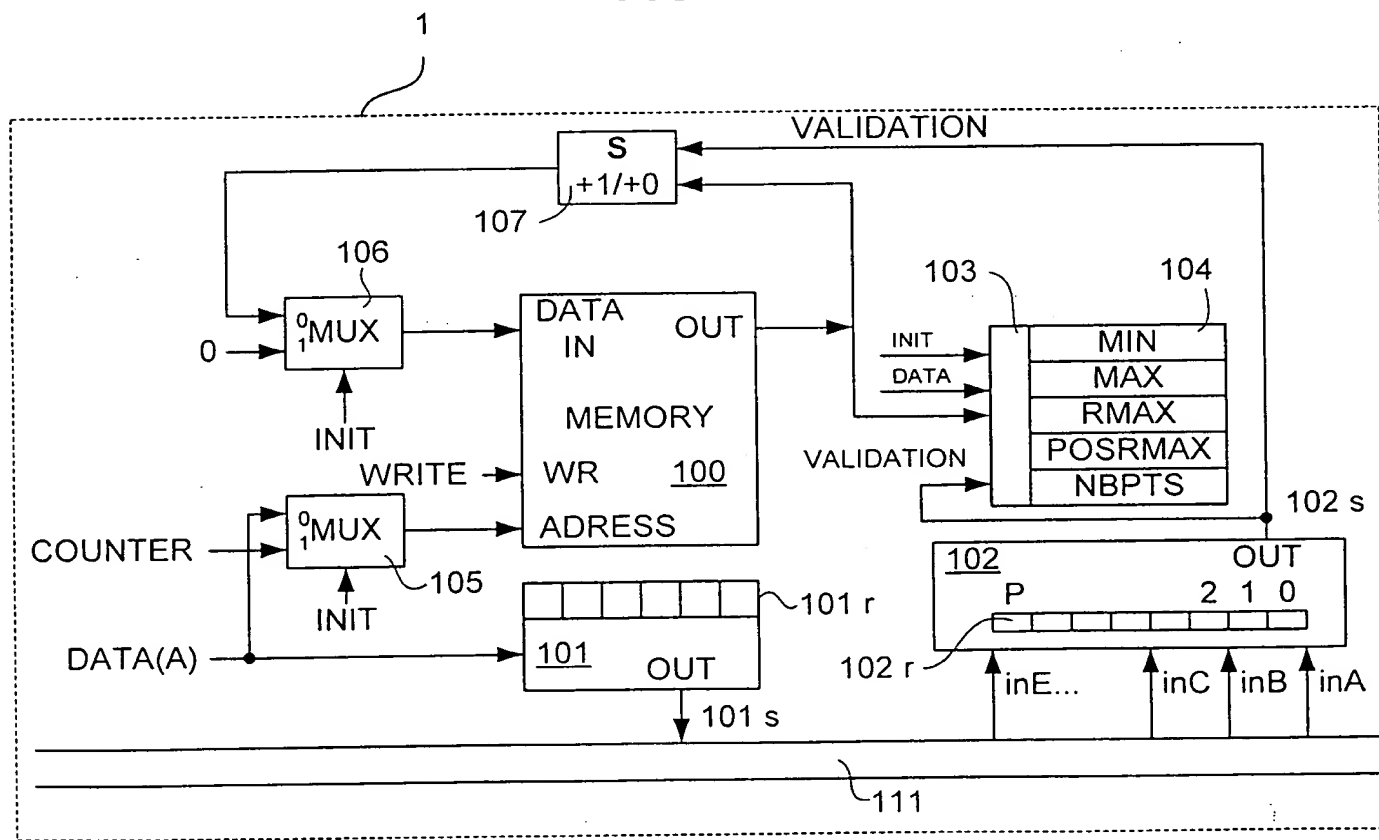


FIG. 3

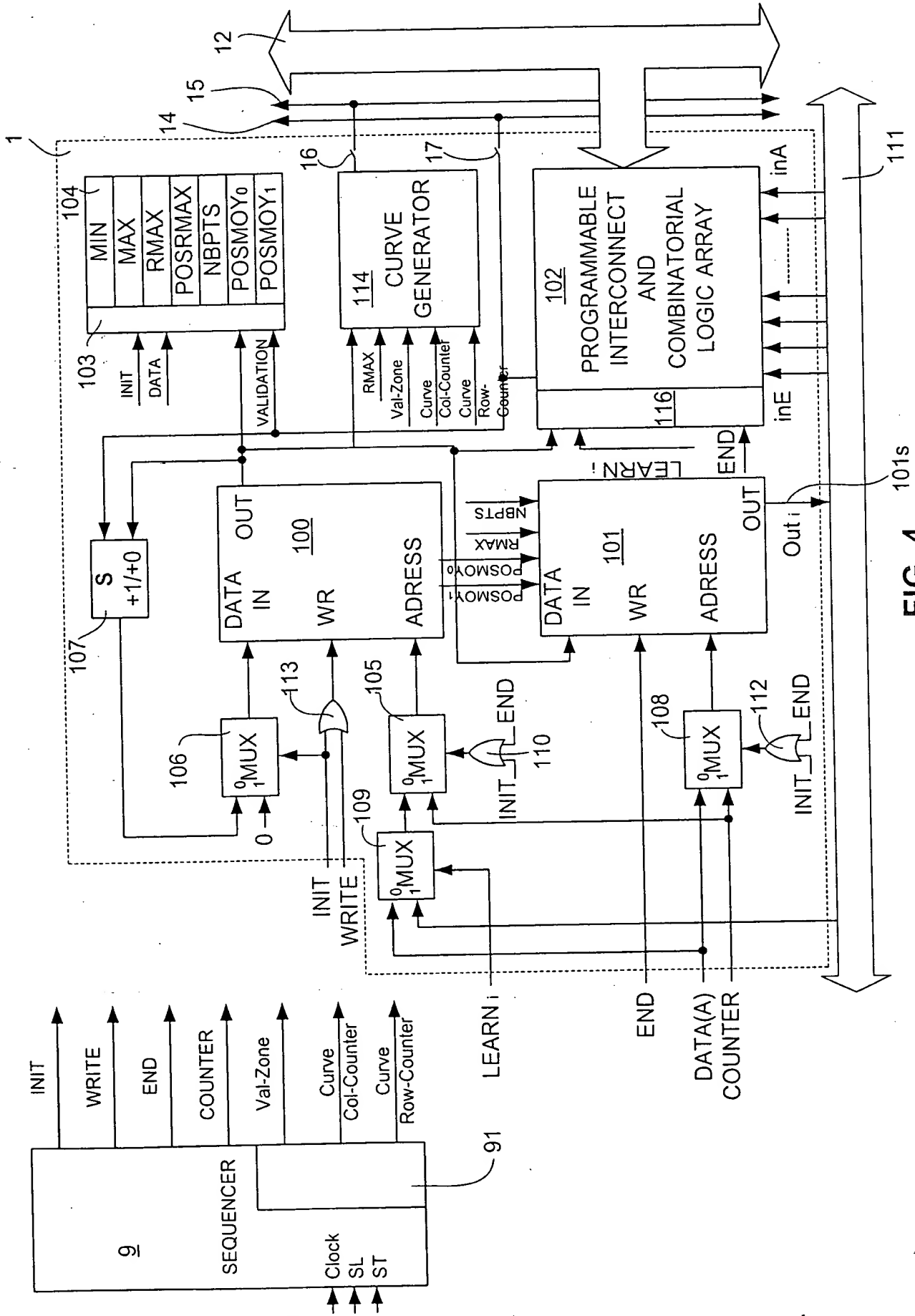
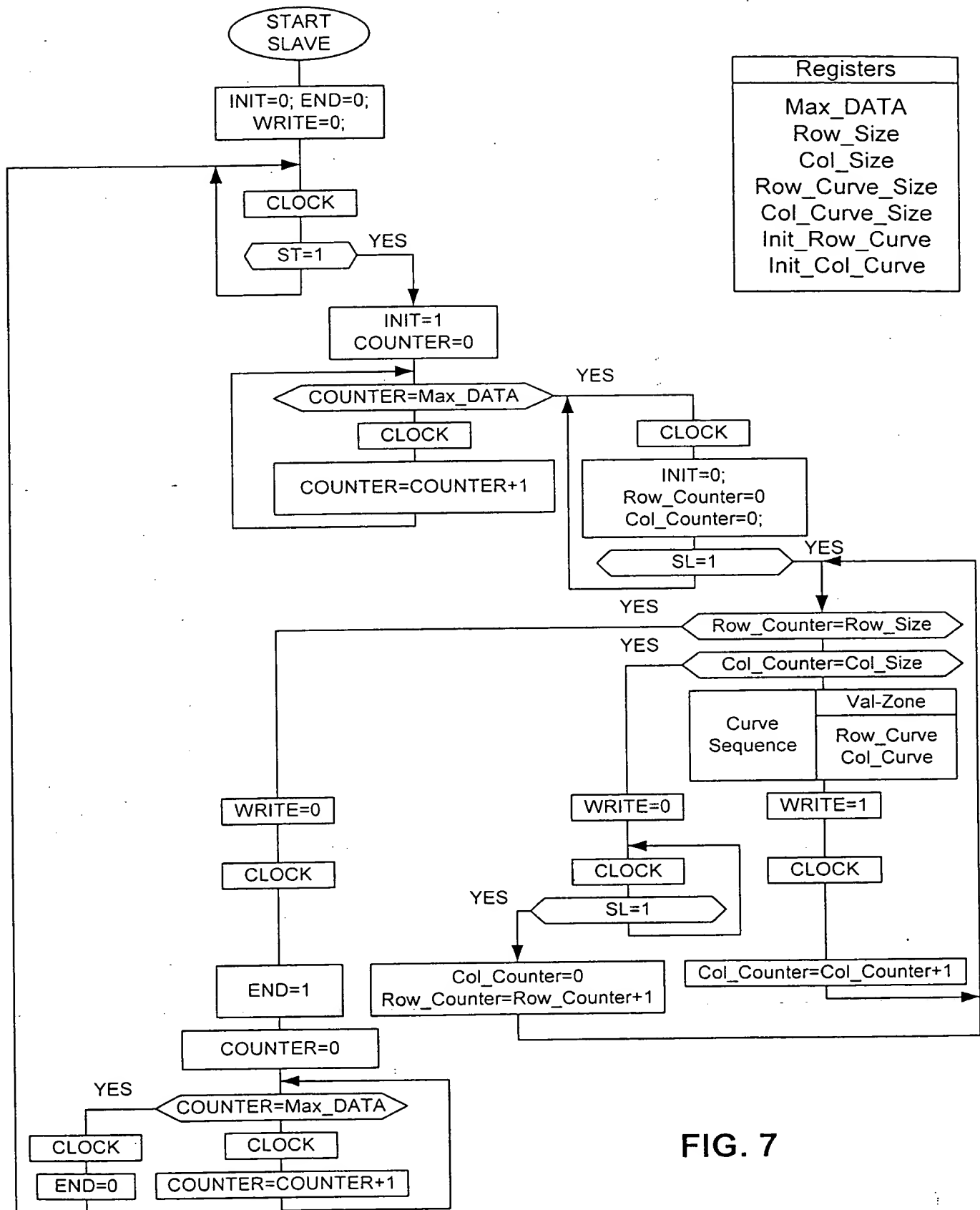


FIG. 4

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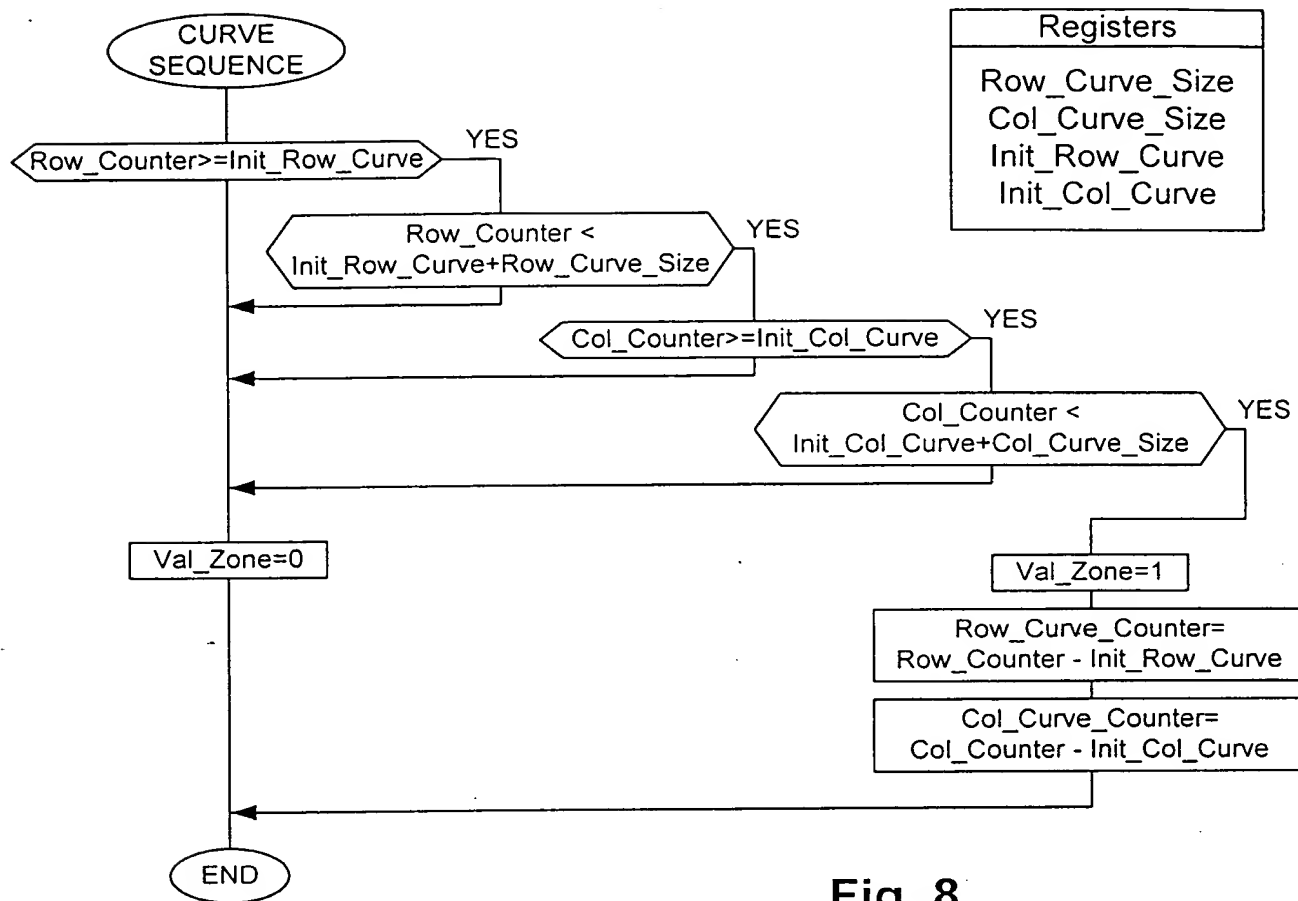


Fig. 8

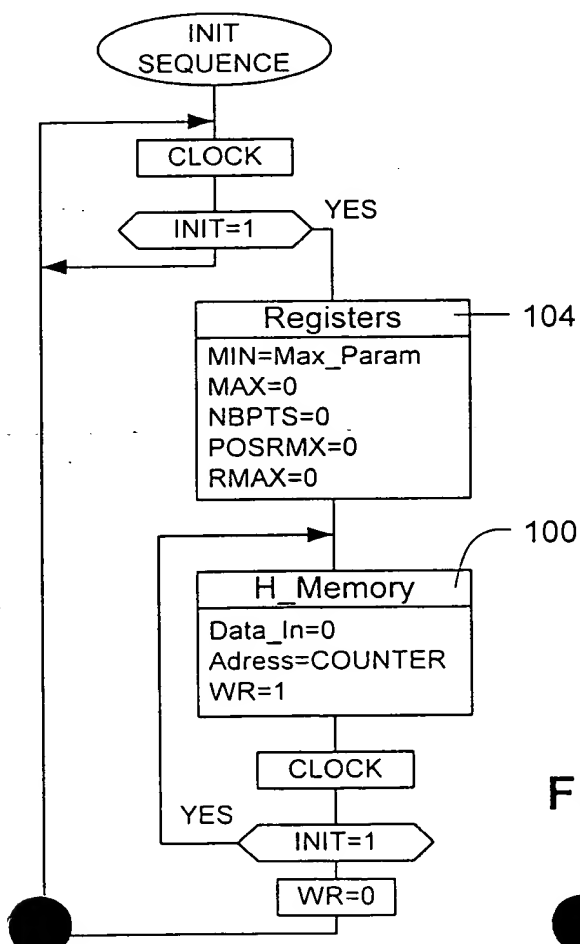


Fig. 9

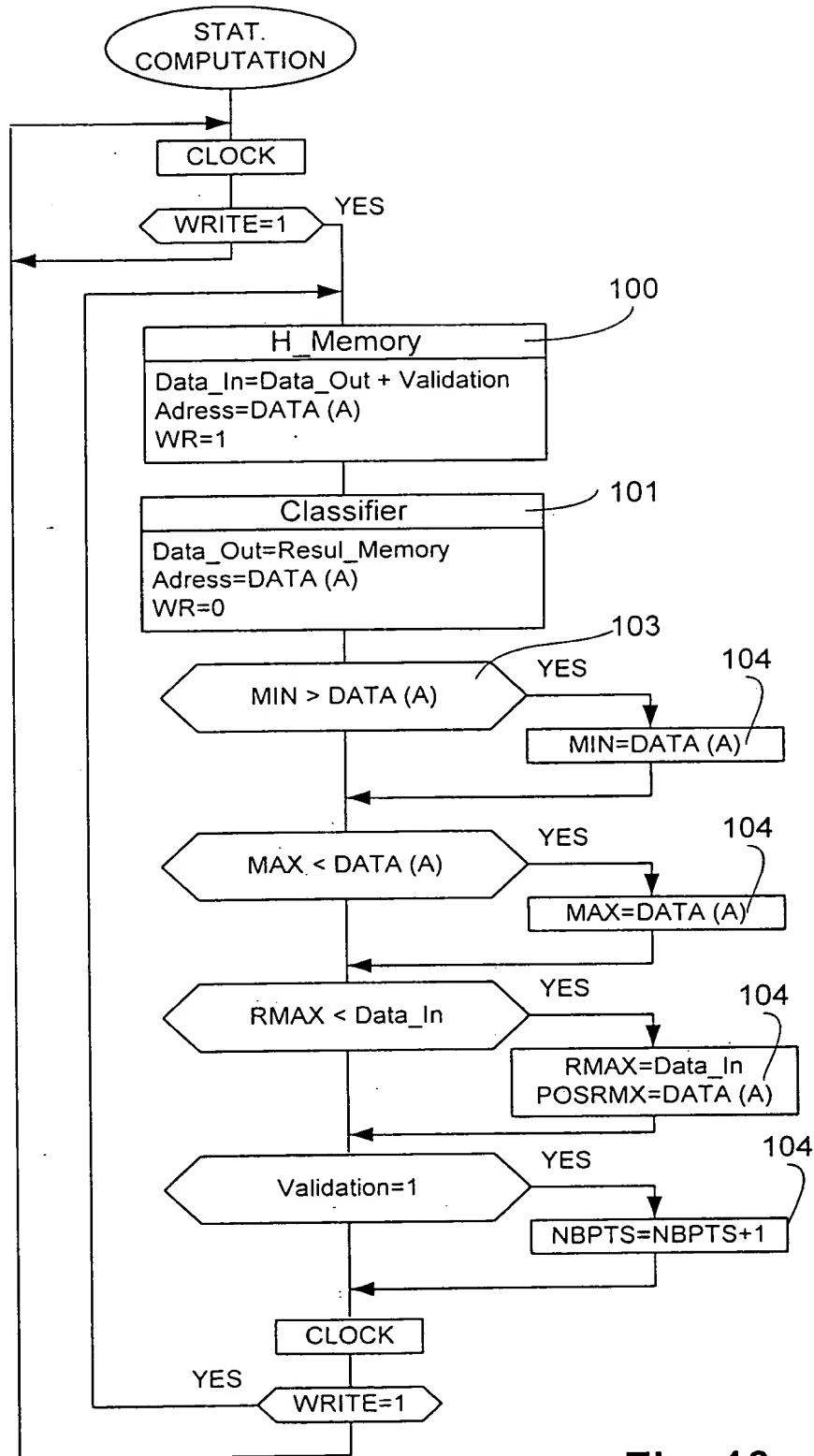


Fig. 10

SECRET

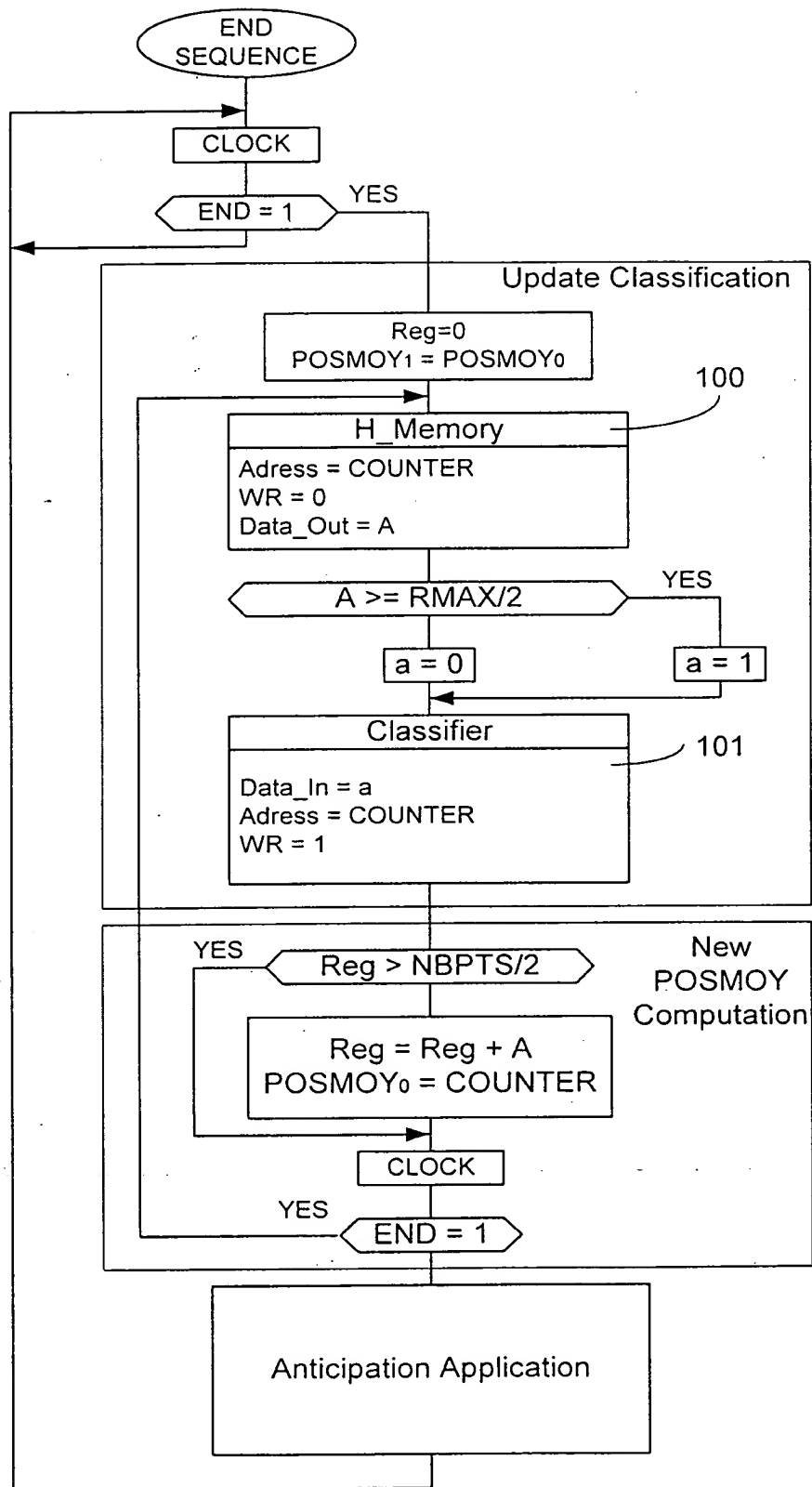
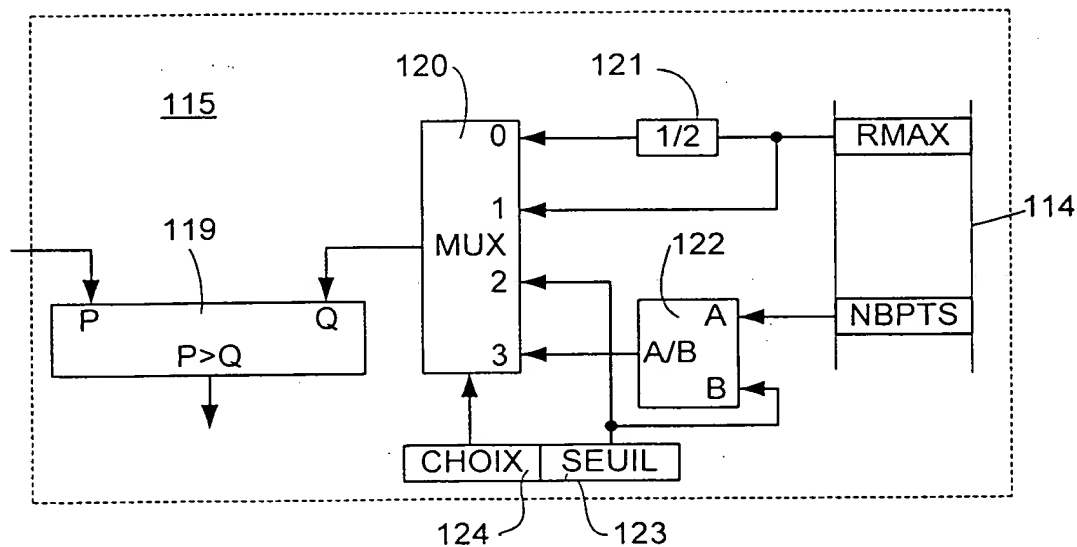


Fig. 11

FIG. 12 is a block diagram of a memory system. It features two memory units, 100 and 118, each with DATA IN, OUT, MEMORY, WR, and ADDRESS ports. Memory unit 100 is connected to a MUX (105) which receives DATA (A) COUNTER inputs. The MUX output goes to the ADDRESS port of memory unit 100. An OR gate (113) combines INIT and WRITE signals to control the WR port of memory unit 100. Memory unit 118 is connected to a MUX (108) which receives DATA (A) COUNTER inputs. The MUX output goes to the ADDRESS port of memory unit 118. An OR gate (112) combines INIT and END signals to control the WR port of memory unit 118. A control logic block (101) contains a 1/2 divider (121), a P>Q comparator (119), and a P register. It also includes a 119s block. The control logic block (101) is connected to a RMAX NBPTS block (104). The output of memory unit 100 is connected to the input of memory unit 118. The output of memory unit 118 is connected to the output of memory unit 100.



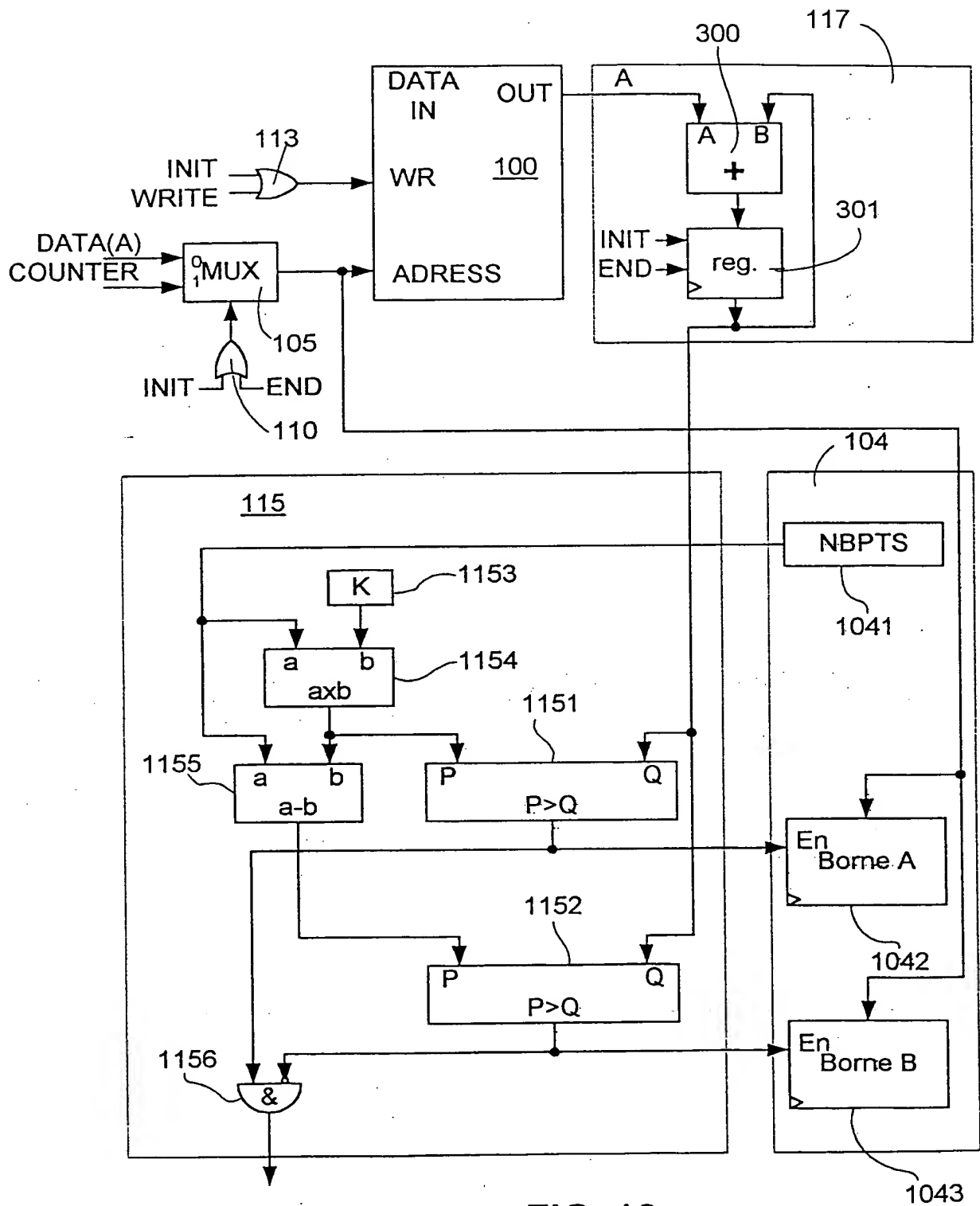
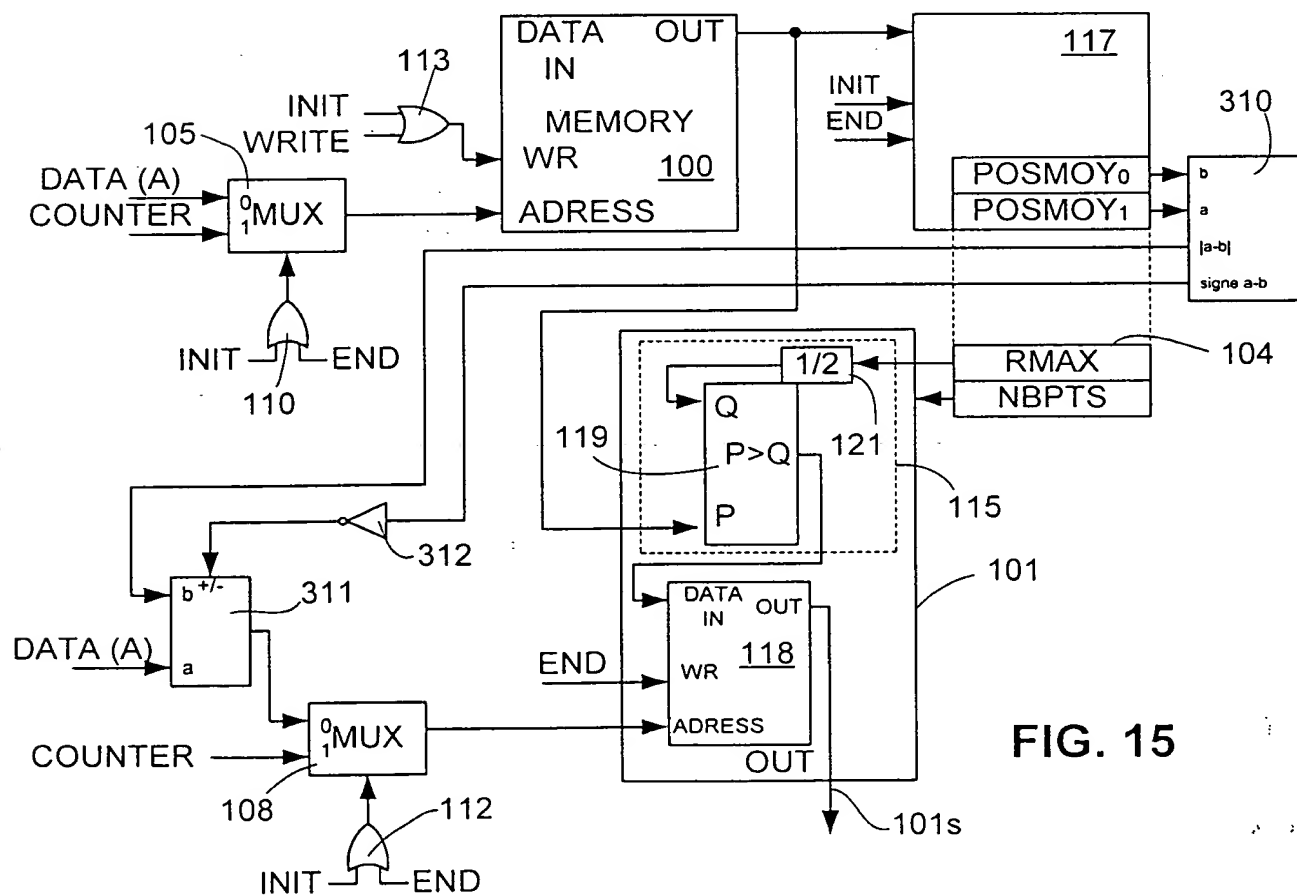
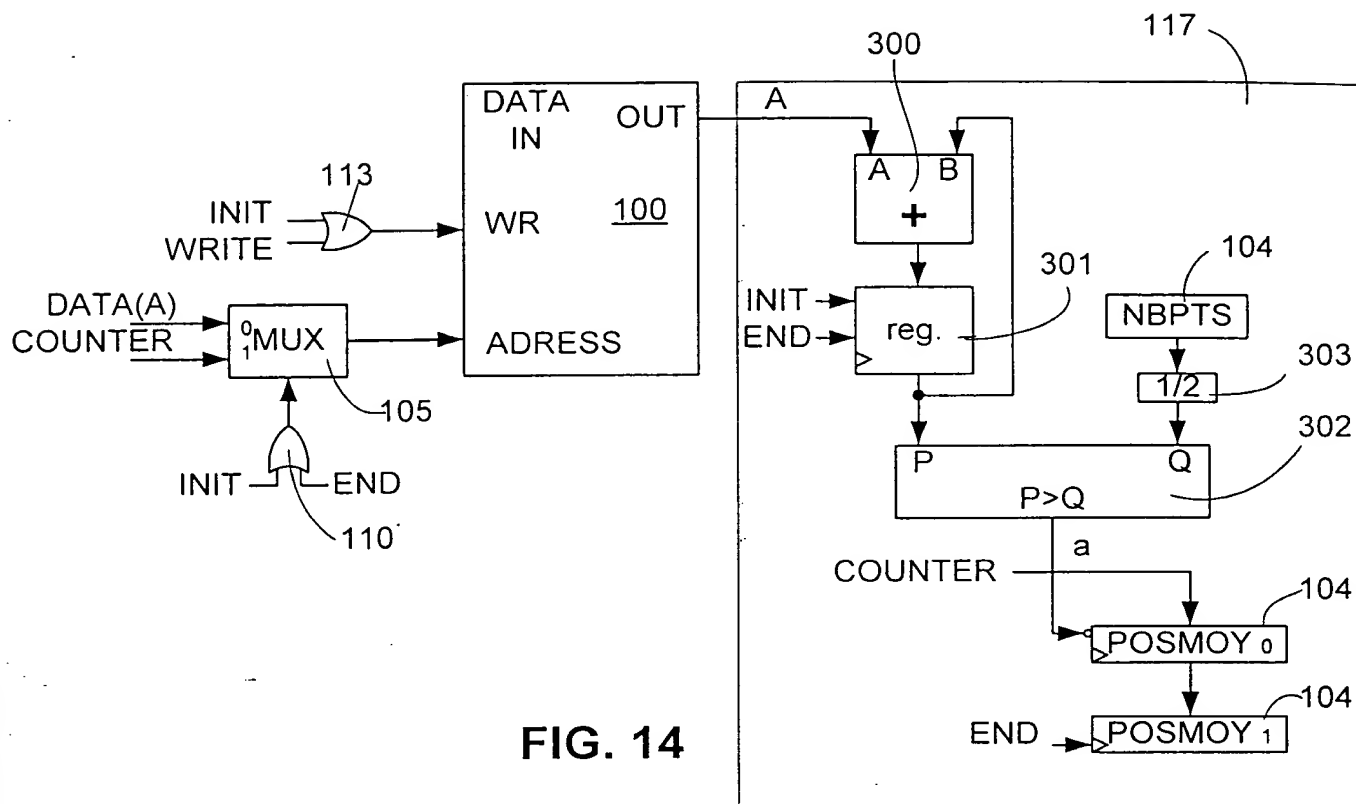


FIG. 13c



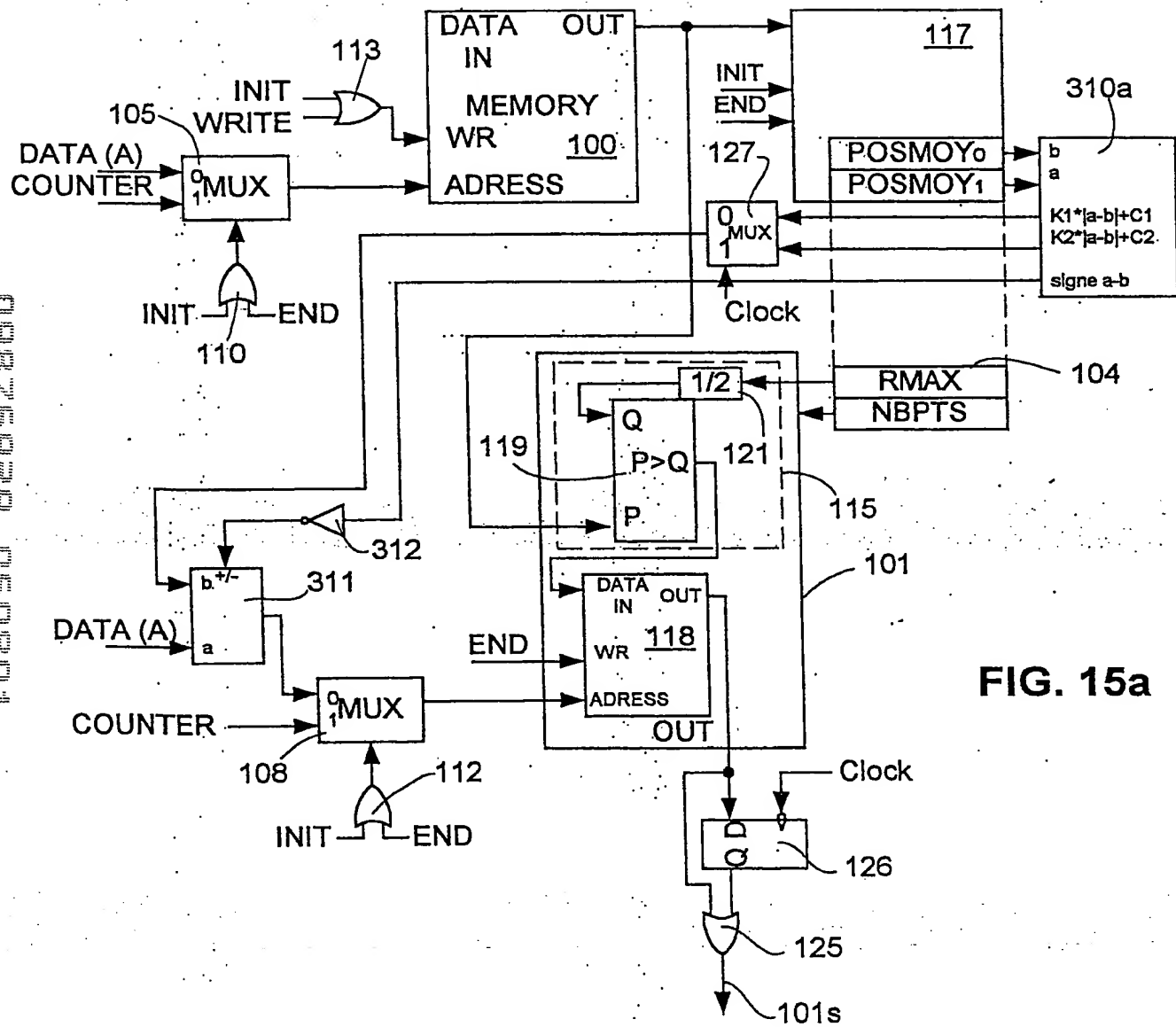


FIG. 15a

FIG. 16

FIG. 16

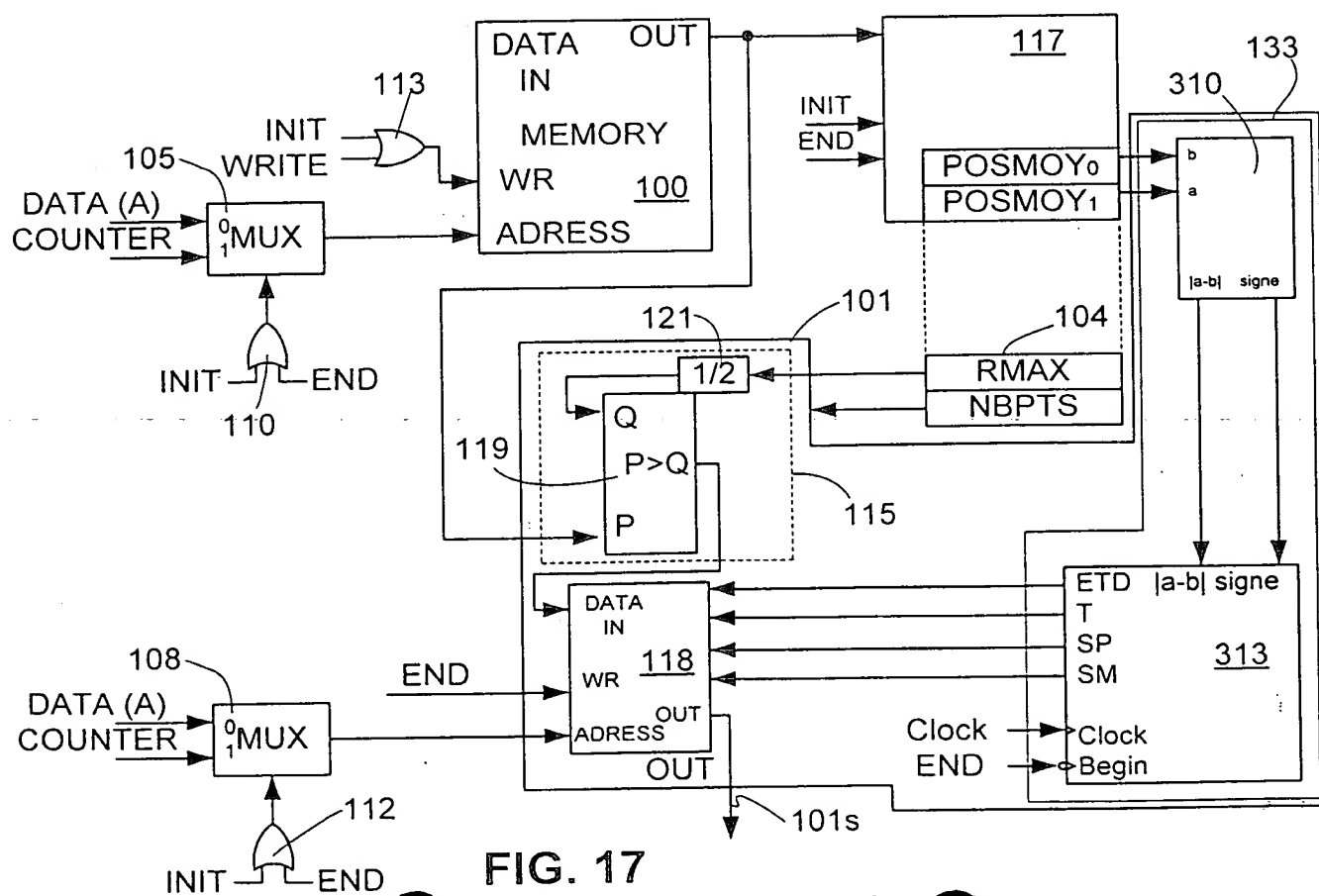
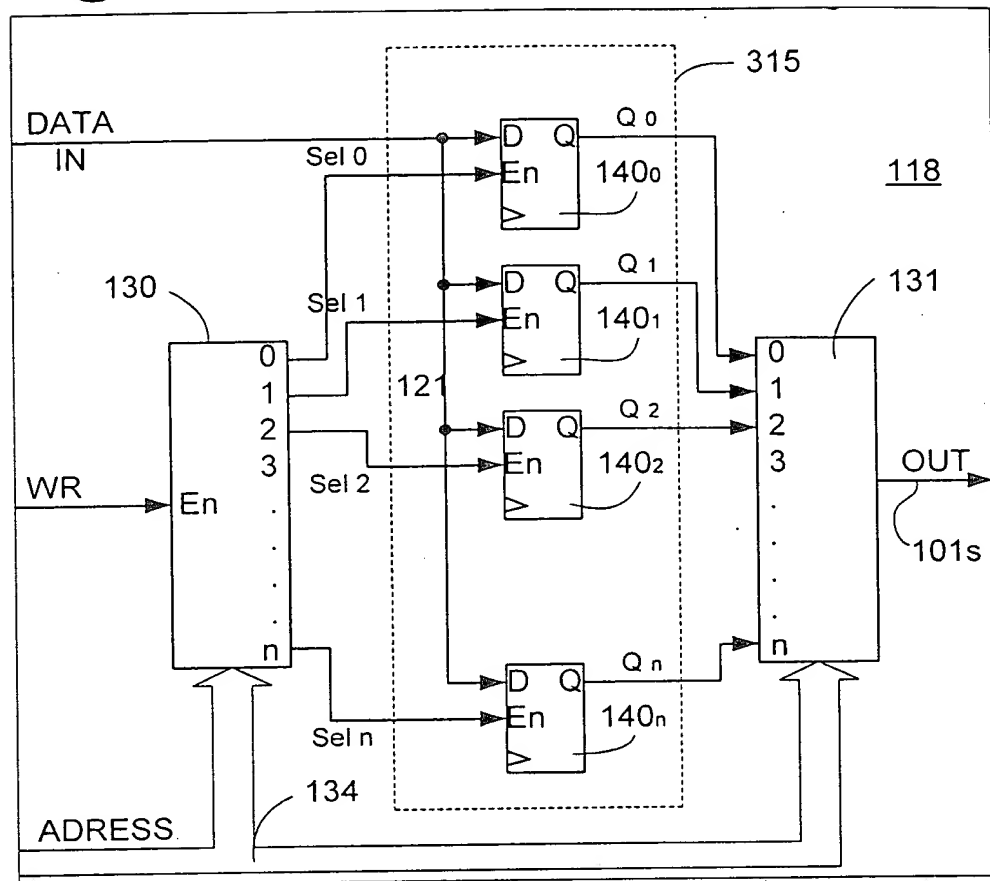


FIG. 17

FIG. 18

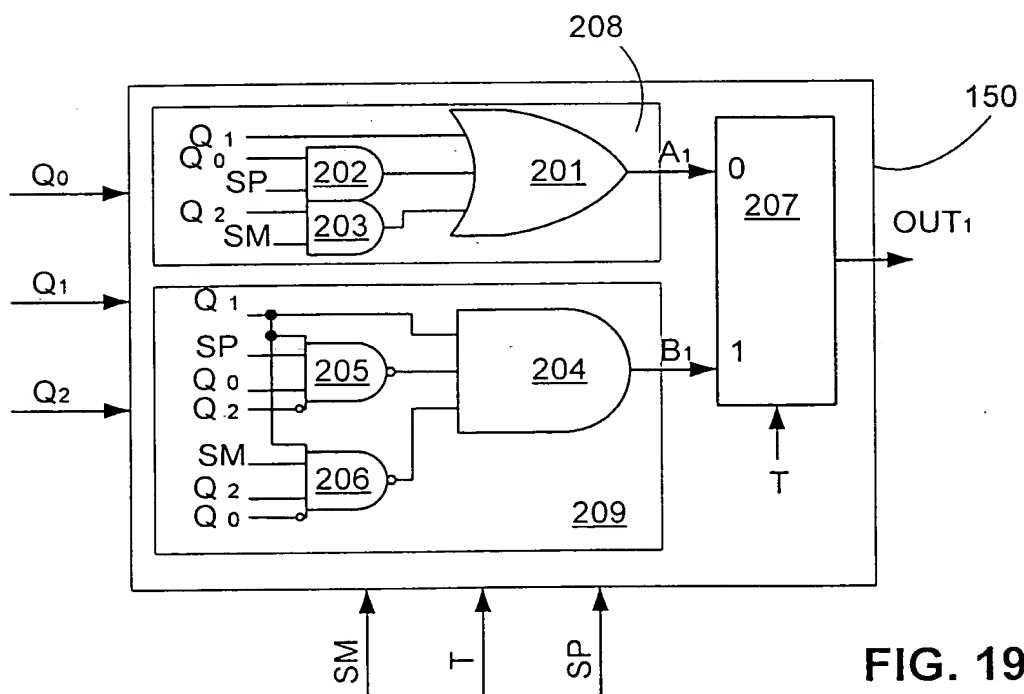
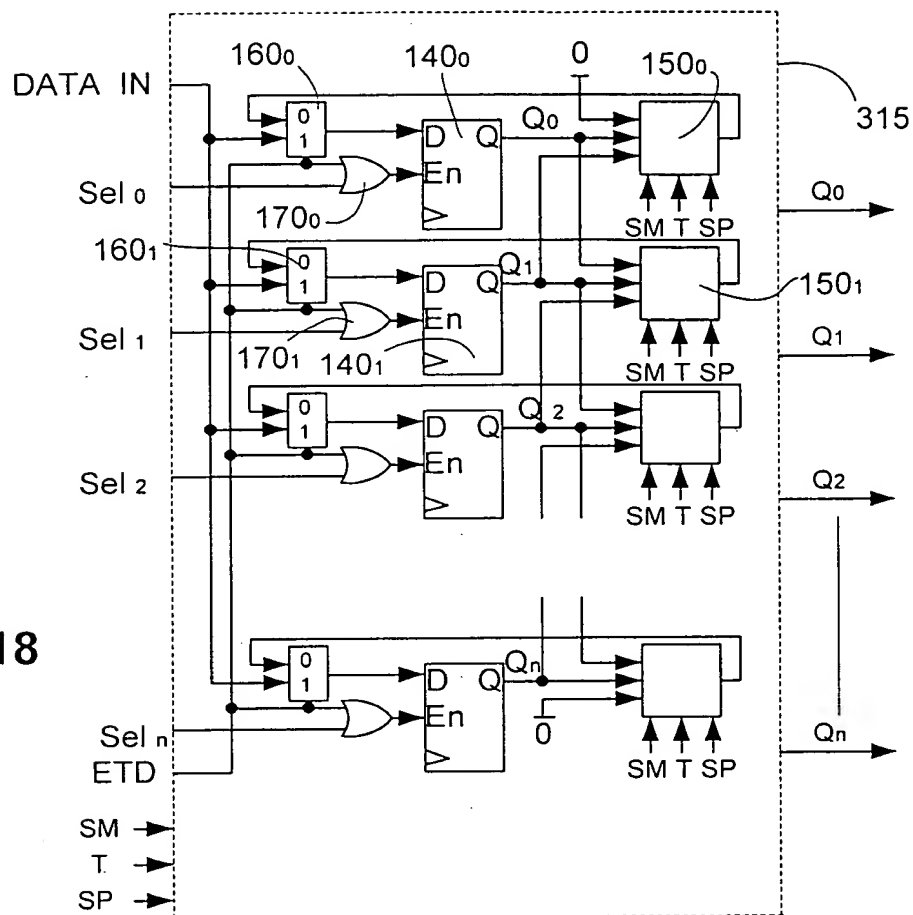


FIG. 19

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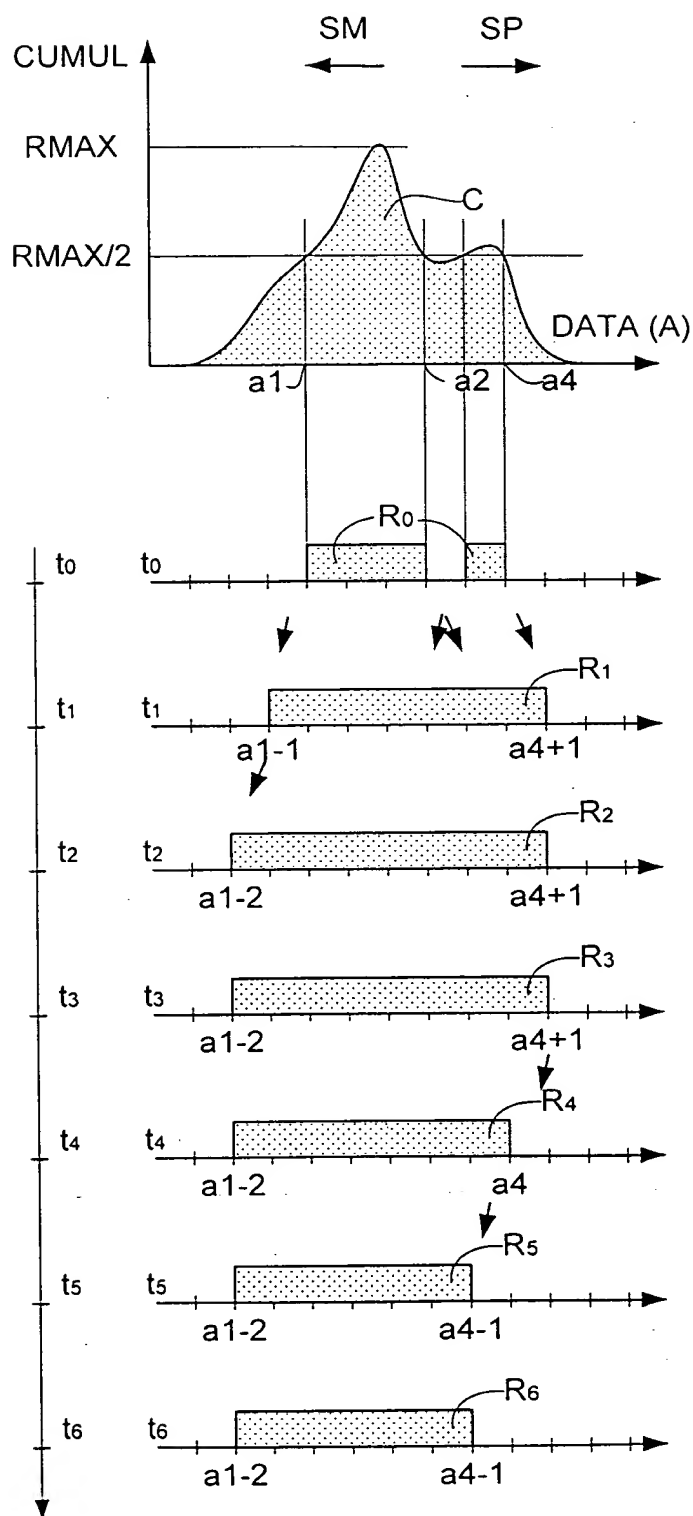
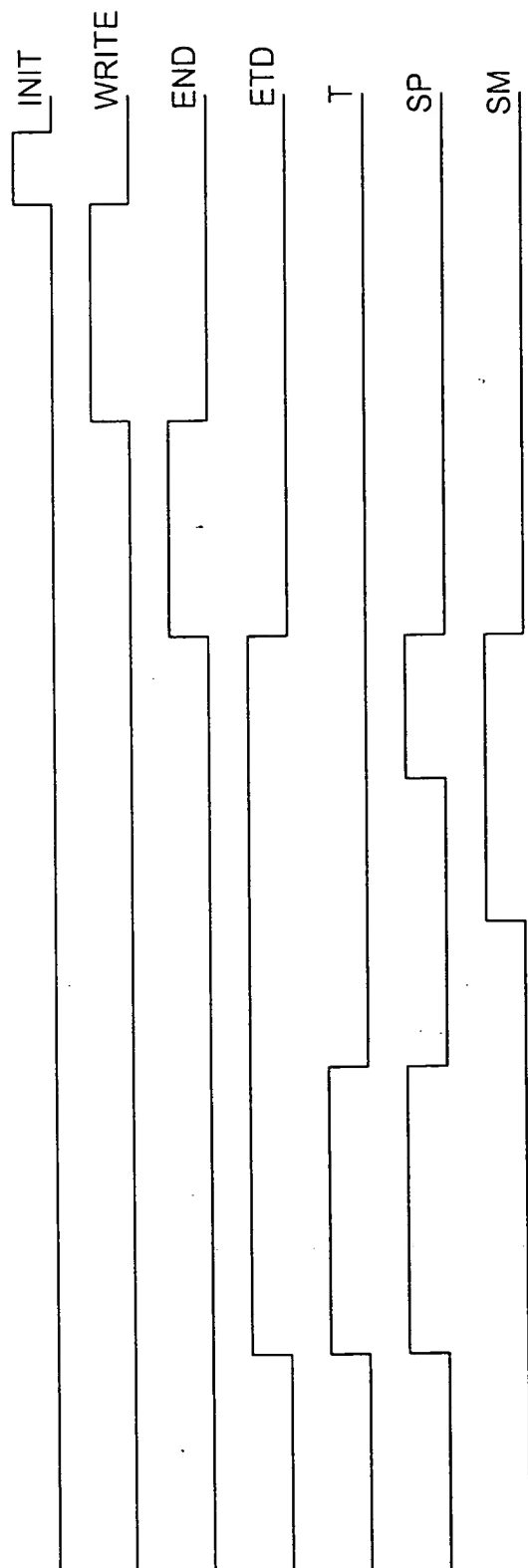


FIG. 20

FIG. 21

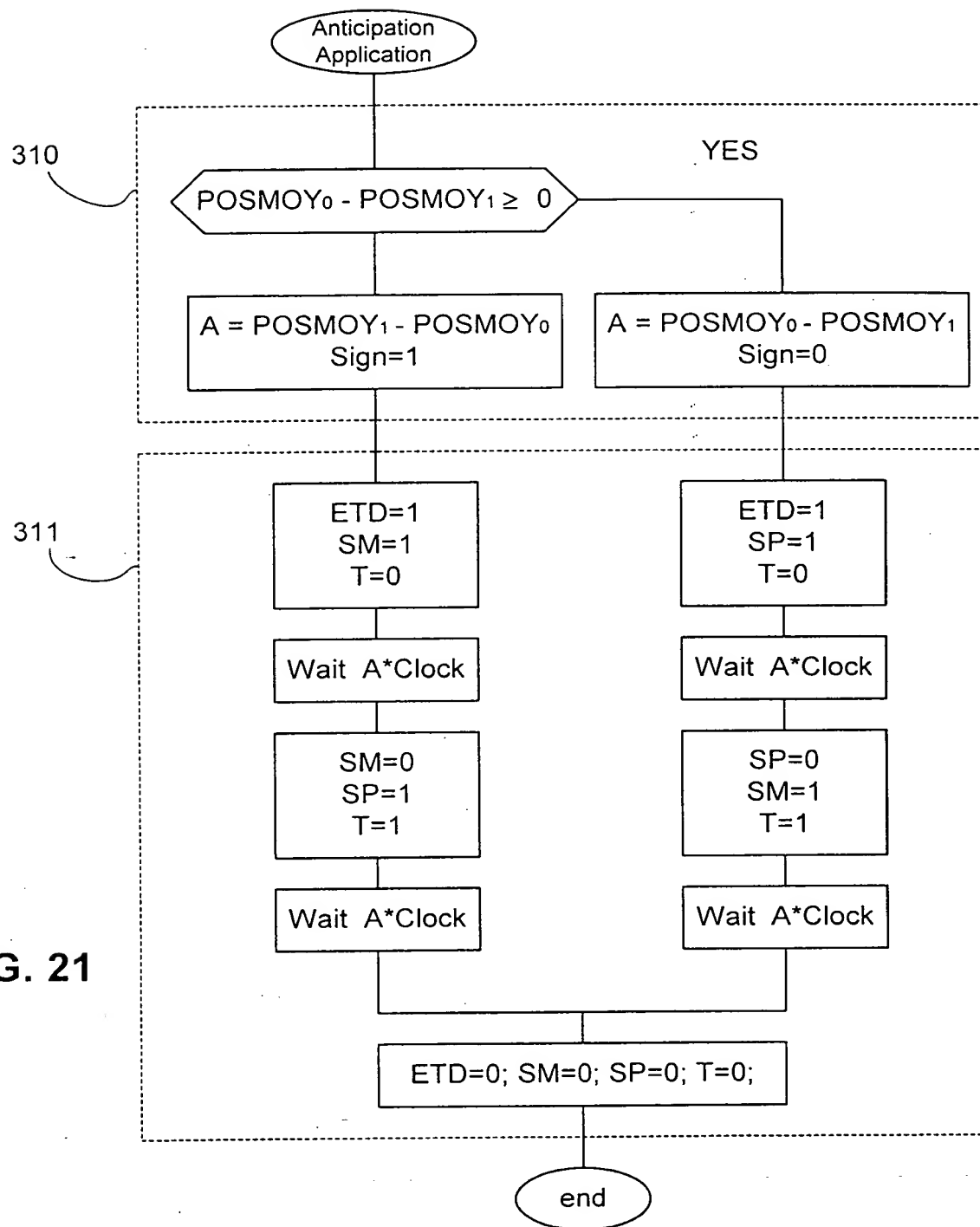


FIG. 22

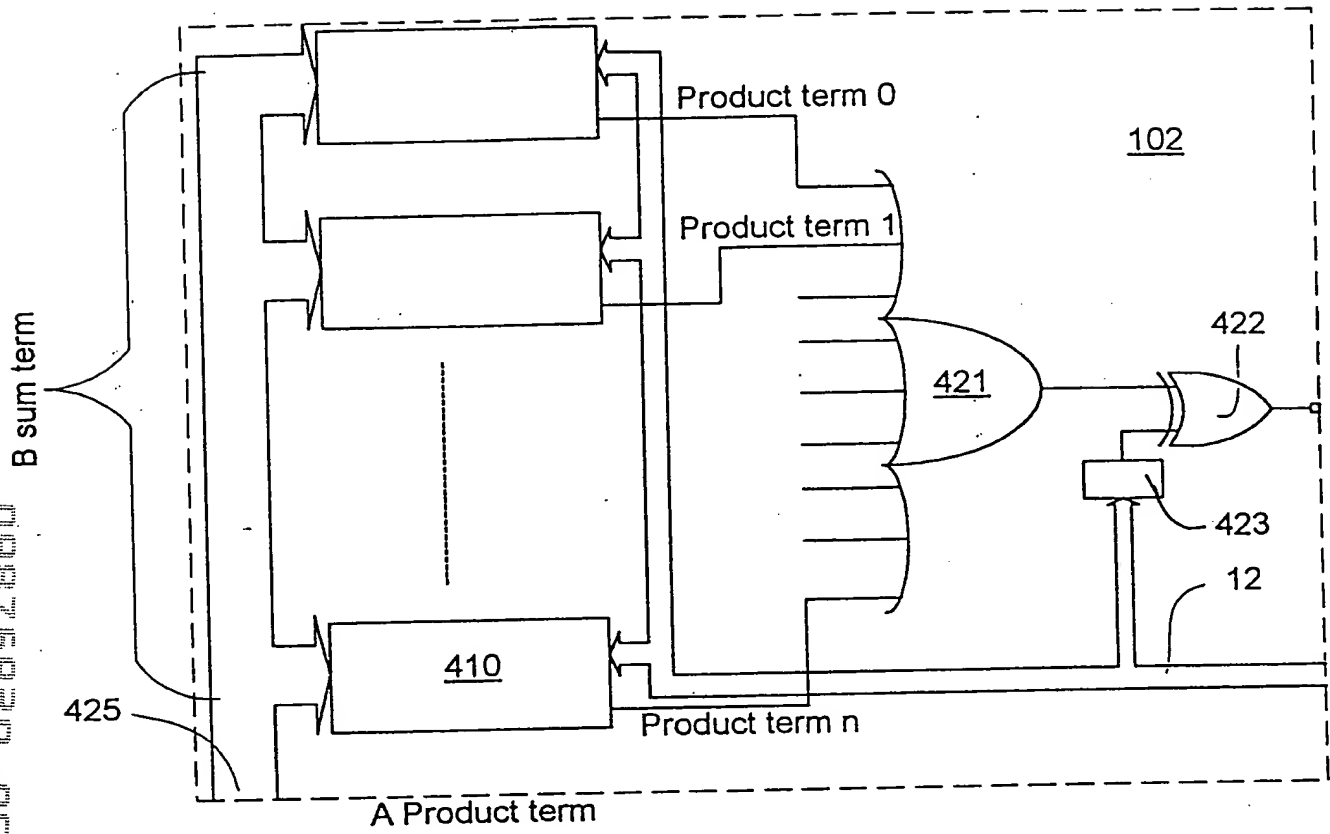


FIG 22

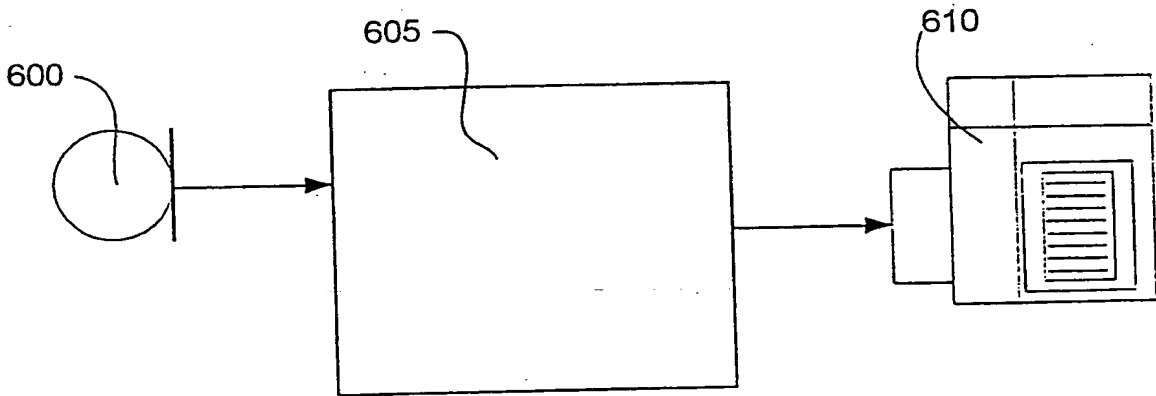


FIG. 39

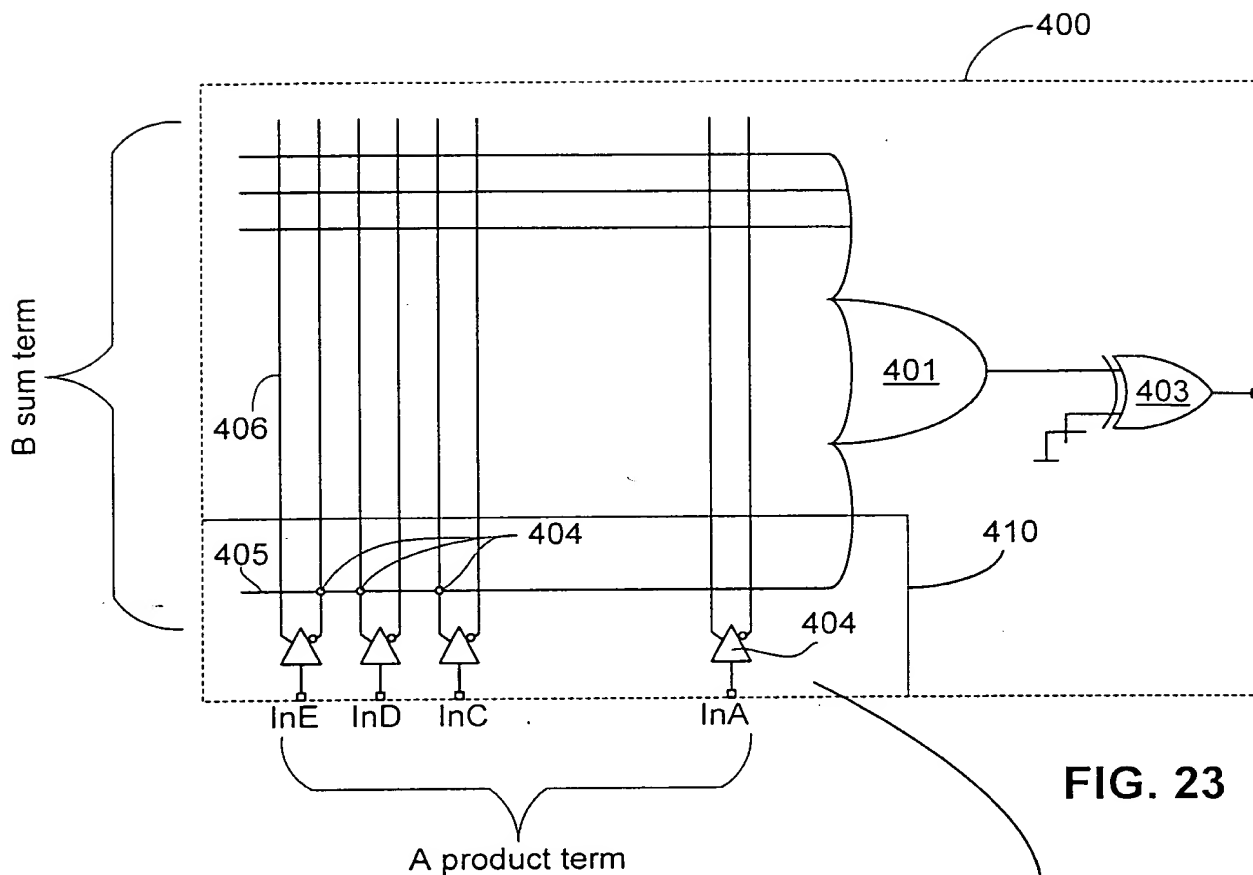


FIG. 23

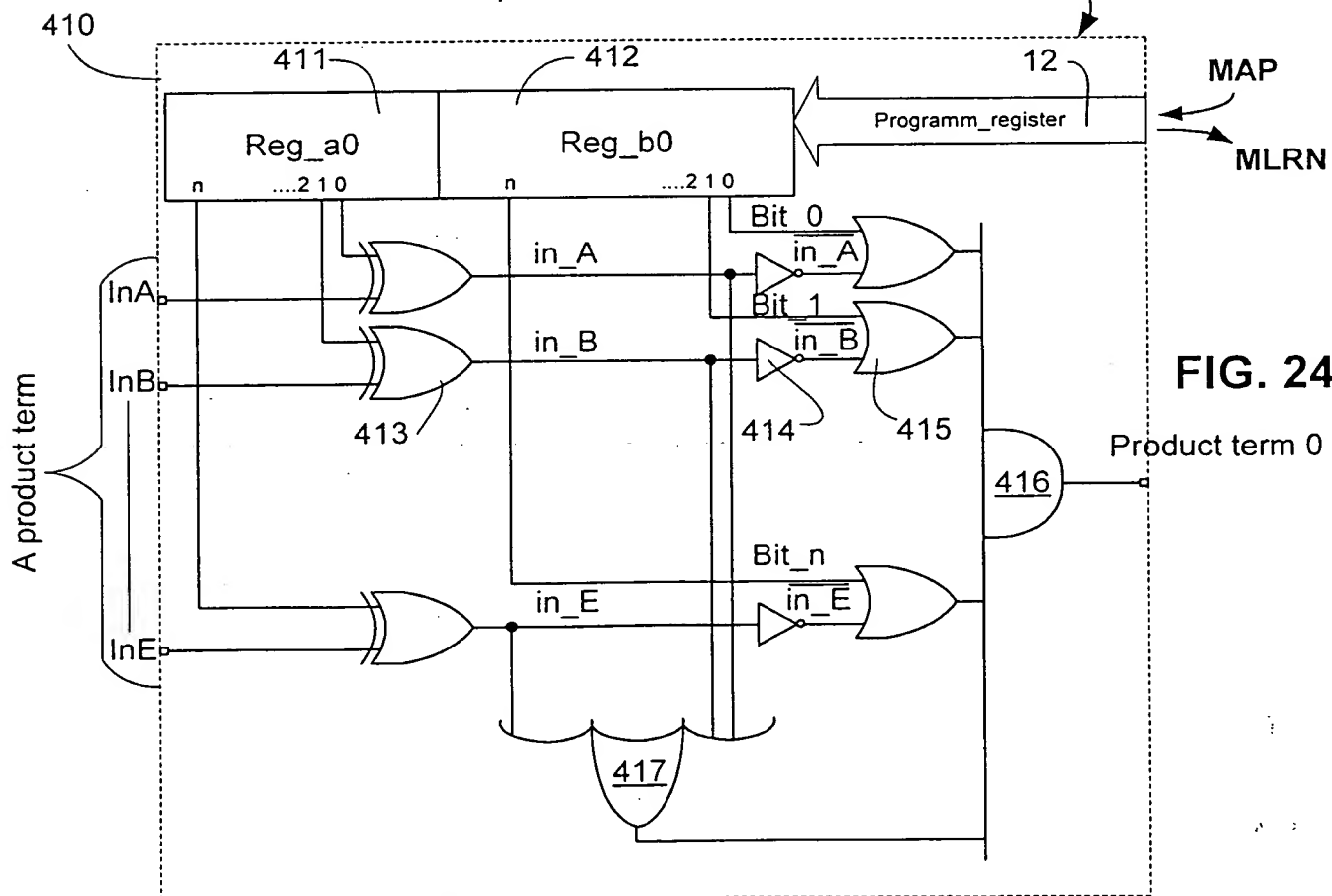


FIG. 24

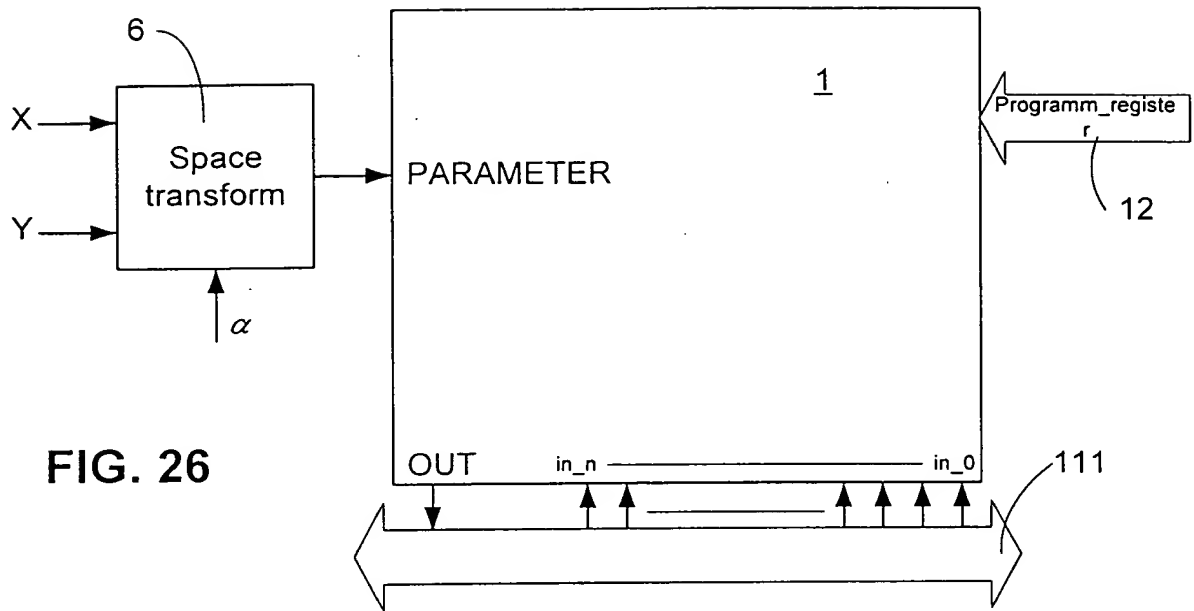


FIG. 26

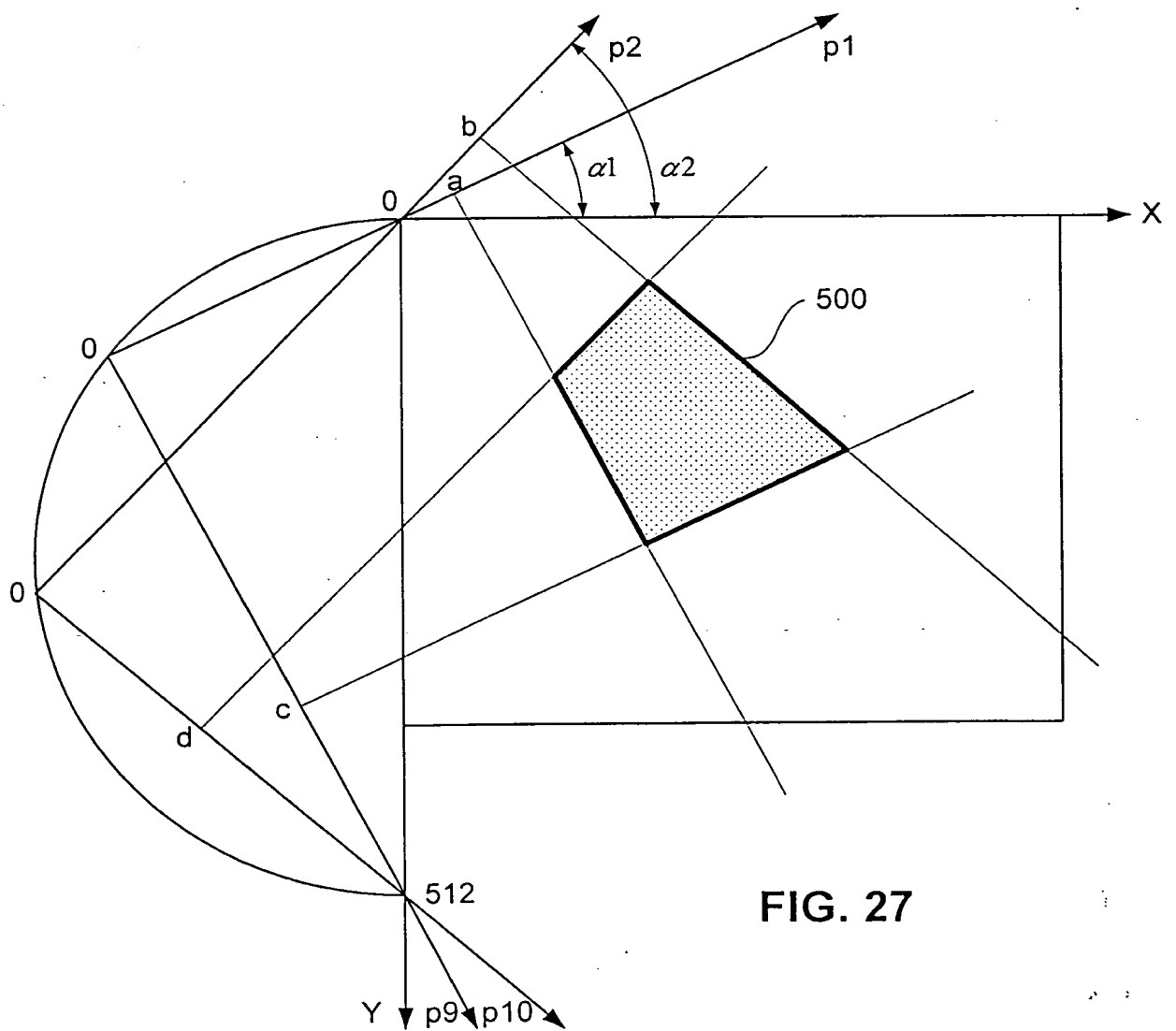


FIG. 27

Fig. 28 is a block diagram of a video processing system. The system includes a memory block (100) with DATA IN, OUT, MEMORY, WR, ADDRESS, and a sequencer block (91) with SV, SH, CLK inputs and a Zone Curve output. A shift register (350) and a flip-flop (351) are connected to the memory and sequencer. A cursor generator (366) and a semi-graphic memory (367) are also shown. The system outputs to a screen (8) via a video signal line (14).

Fig. 28

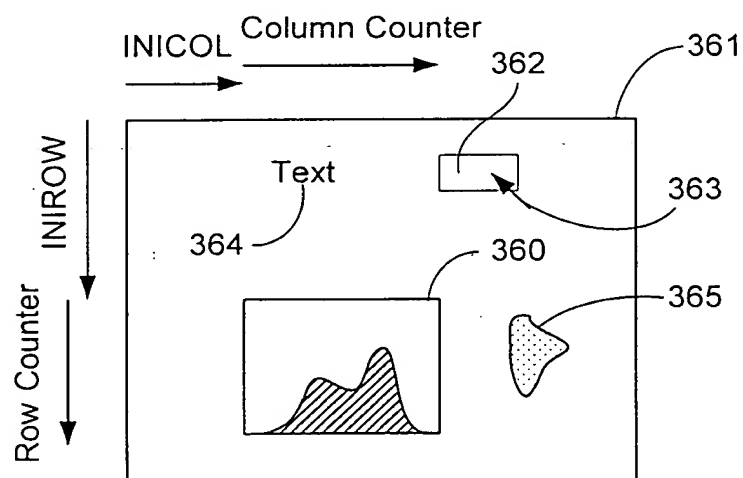


Fig. 29

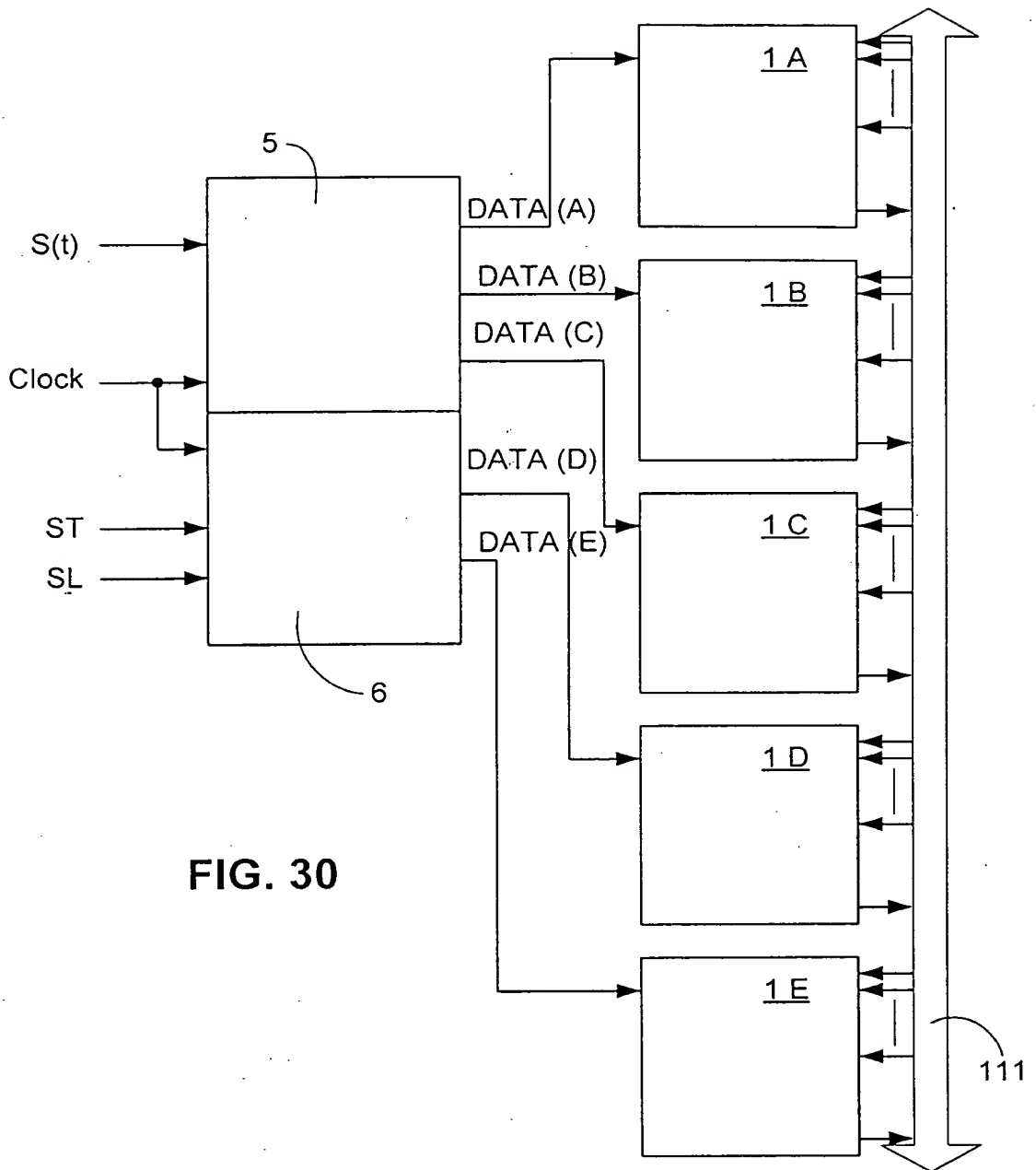
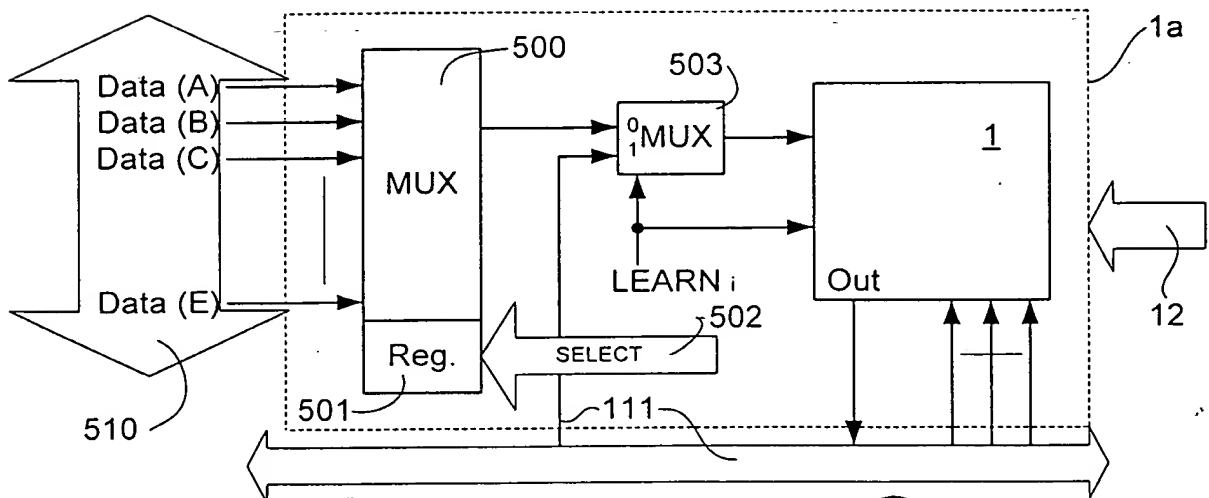


FIG. 30

FIG. 31



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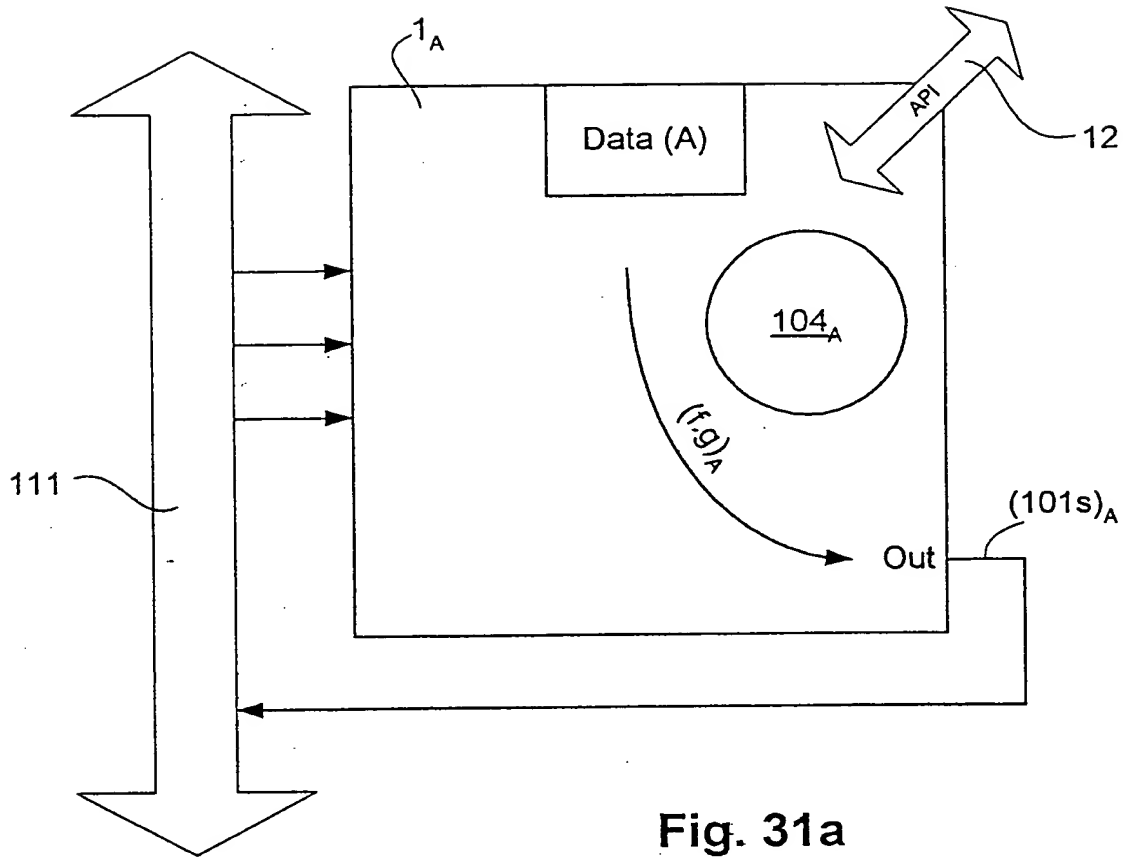


Fig. 31a

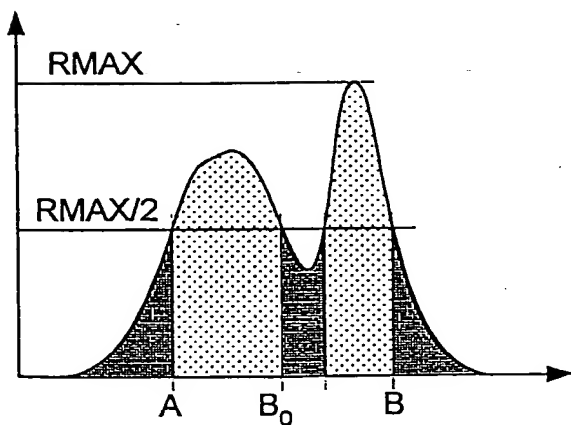


Fig 13a

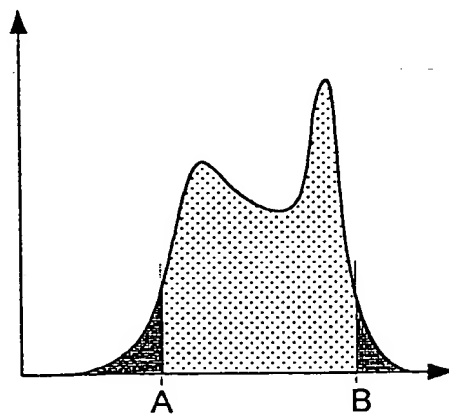


Fig 13b

FIG. 32

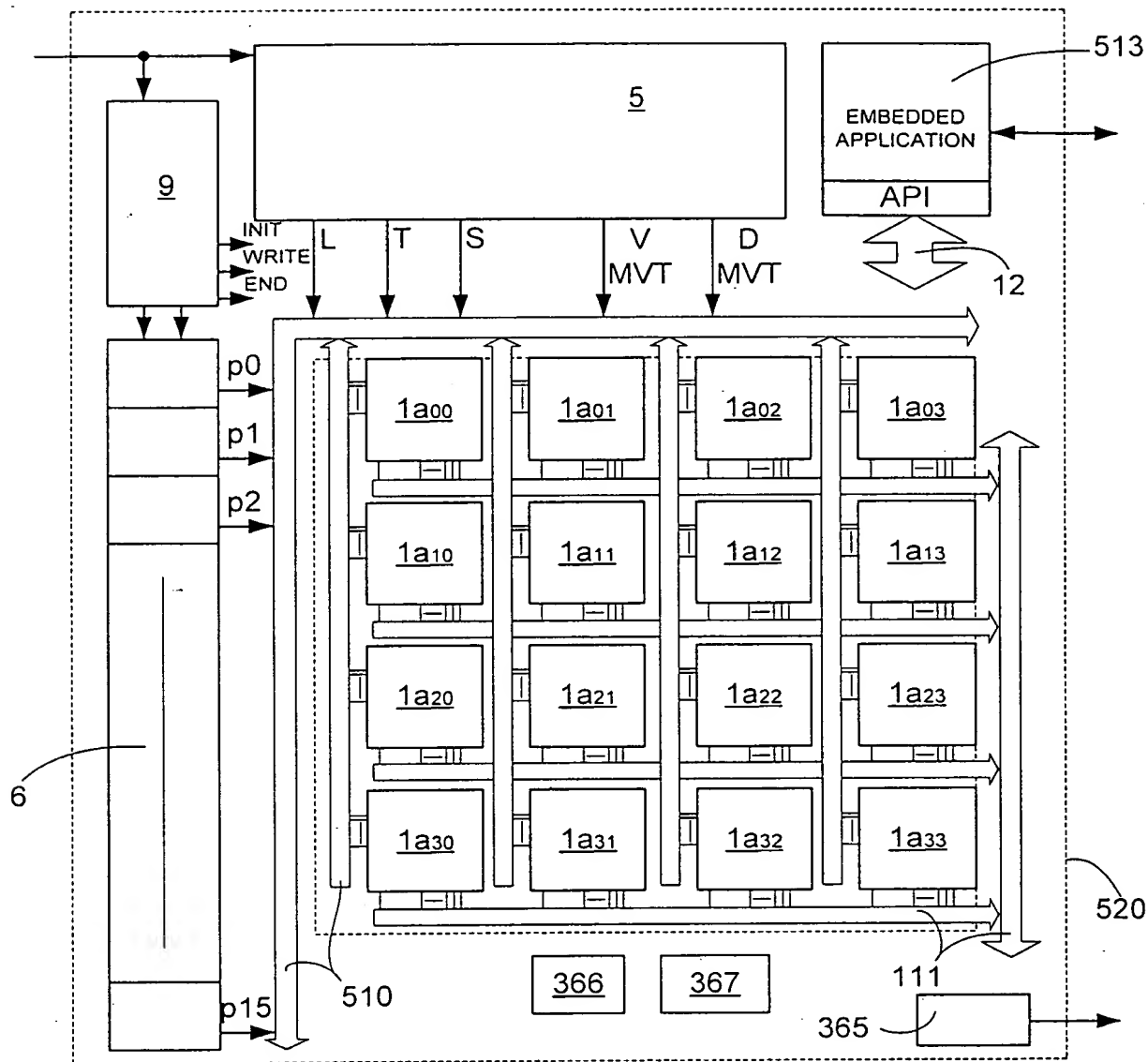


FIG. 32

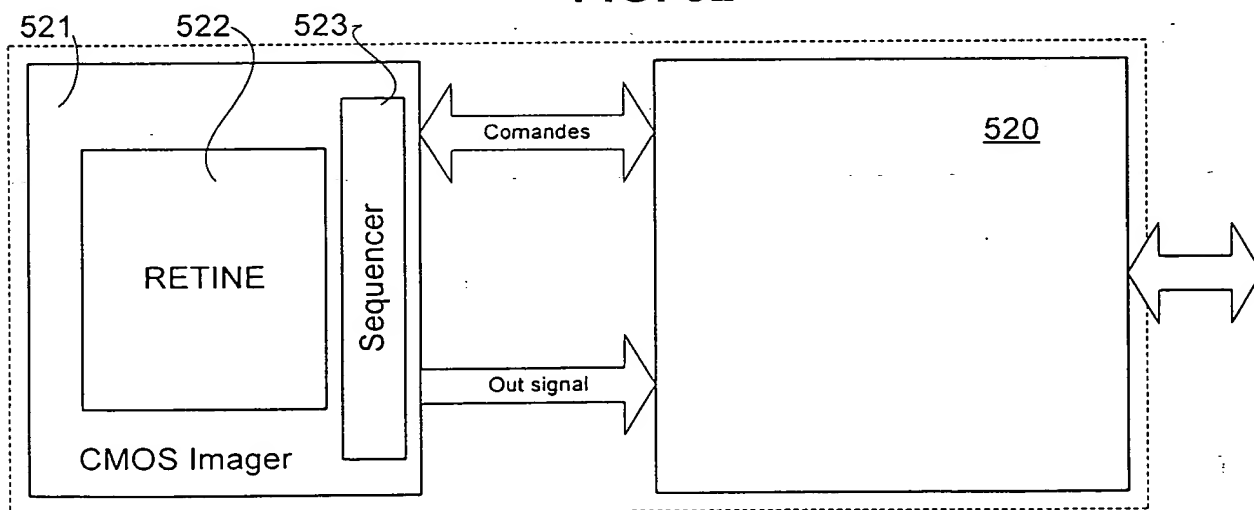


FIG. 33

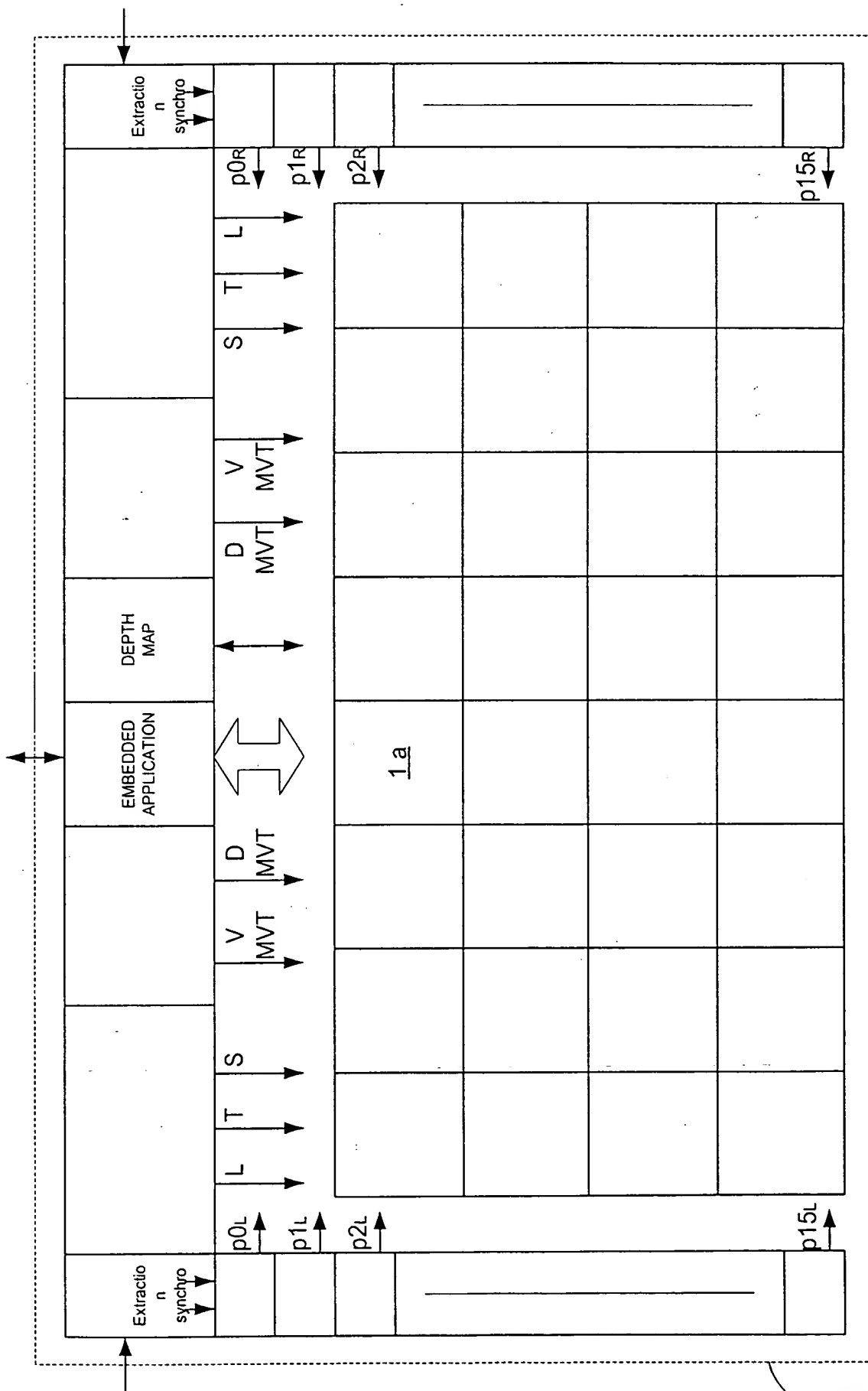


FIG. 34

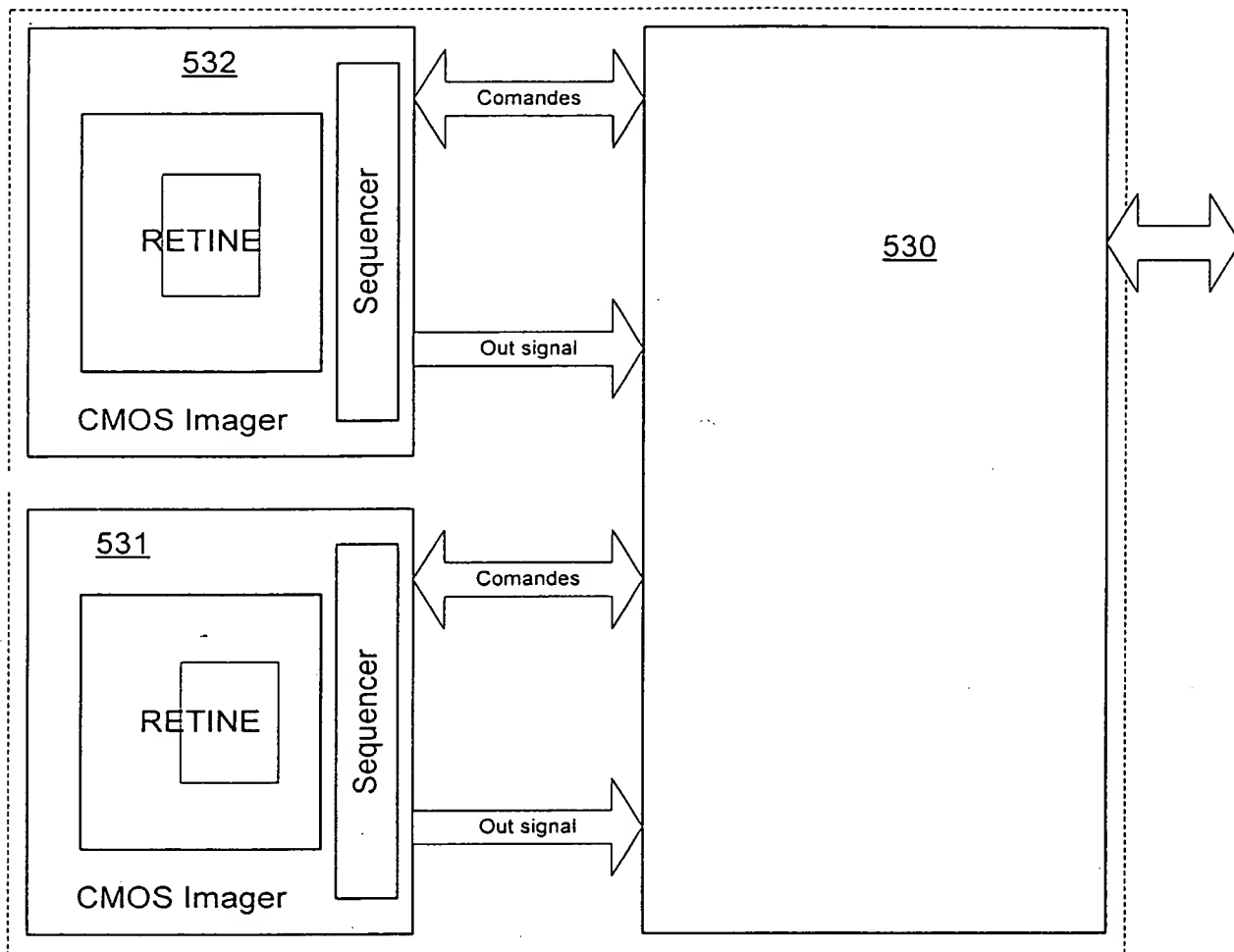


FIG. 35

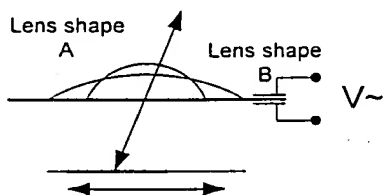
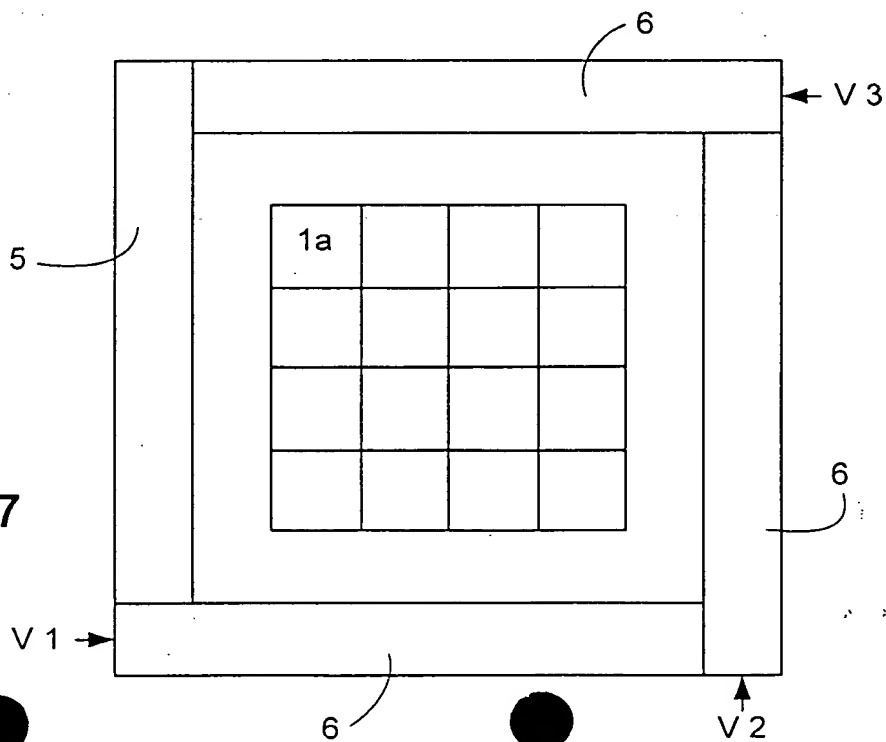


FIG. 36

FIG. 37



The diagram illustrates the system architecture. At the top, a **SCREEN** (8) is connected to a vertical bus (365). A **SR** signal is sent from the bus to the screen. Below the bus, a block (367) receives **DPDATA** and **CLRSCR** signals and sends data to the bus. Another block (366) receives **DPNTER** and sends data to the bus. The bus (365) is connected to a block (15) which has bidirectional connections (14) to the bus. The main system block (1a) contains an **A.P.I.** (Application Programming Interface) and several internal components. It receives **DATA (A)**, **DATA (B)**, and **DATA (E)** from a source (510). It also receives **SELECT** and **LEARN** signals. Inside the block, there is a **GET** block, a **START** block, a **STOP** block, a **MAP** block, and an **MLRN** block. The **CLCURV**, **AFCURV**, **AFMAP**, and **CLMAP** signals are sent from the internal components to the bus. The **Out(i)** signal is sent from the block to the bus. The entire system is labeled (111).

-111

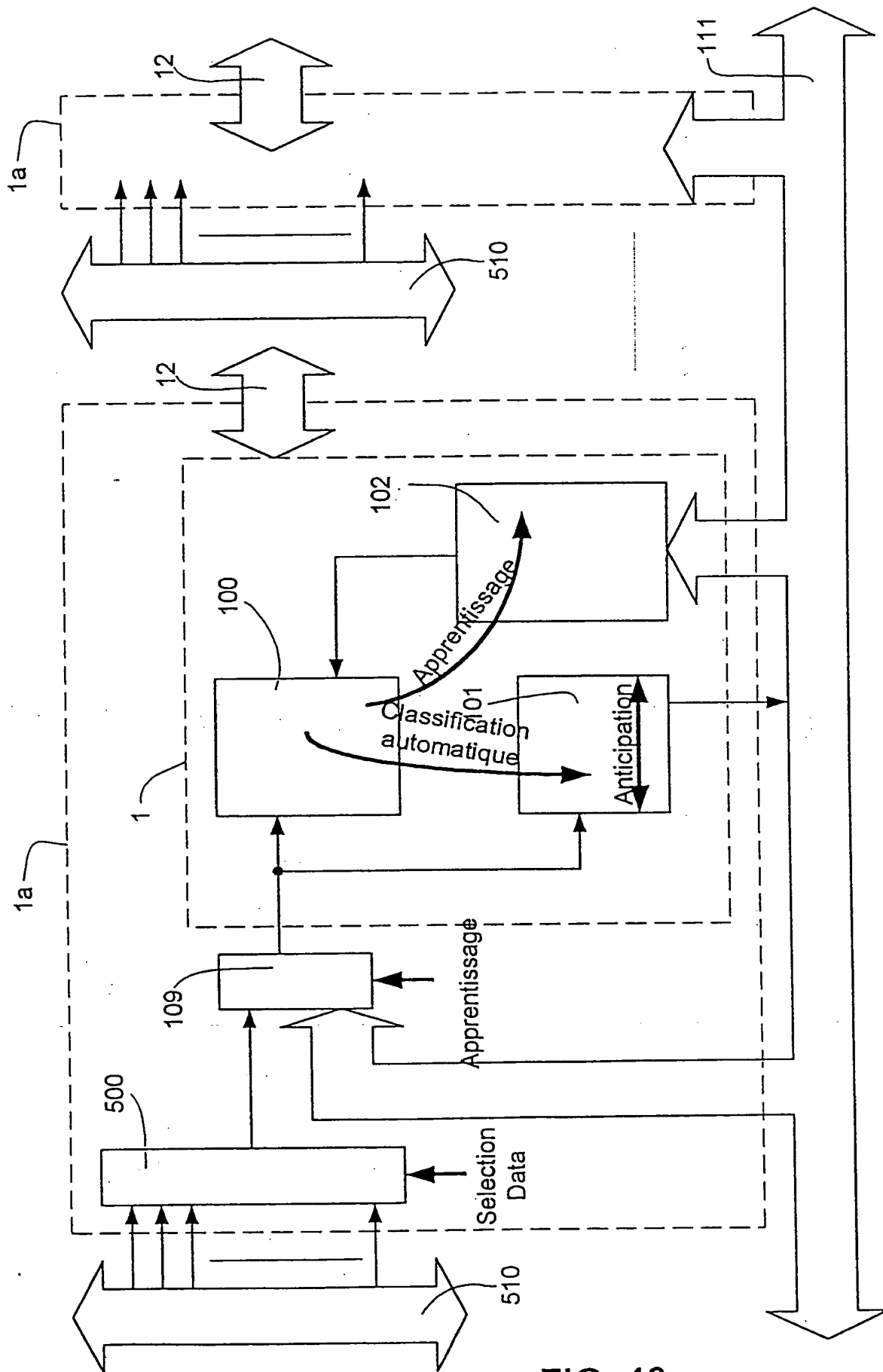


FIG. 40

FIG. 41

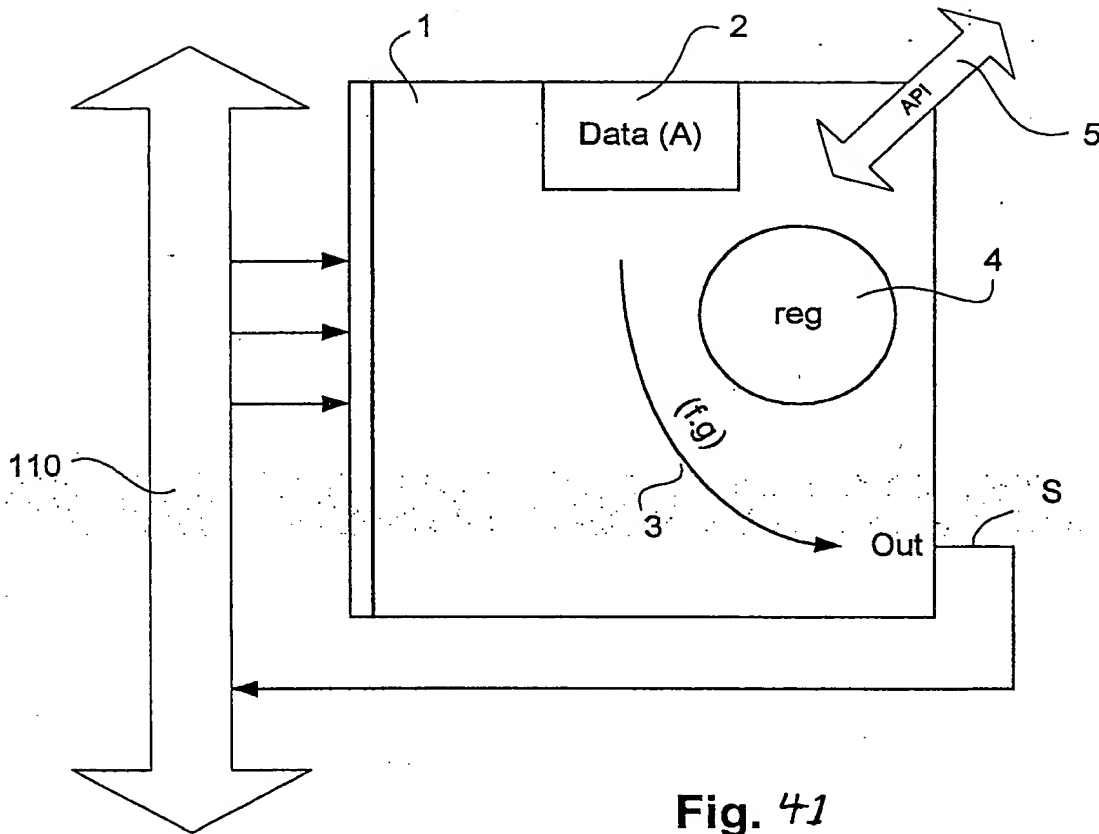
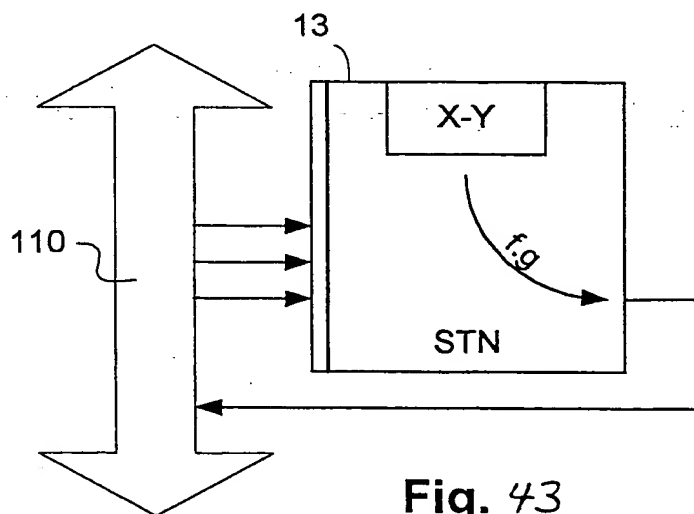
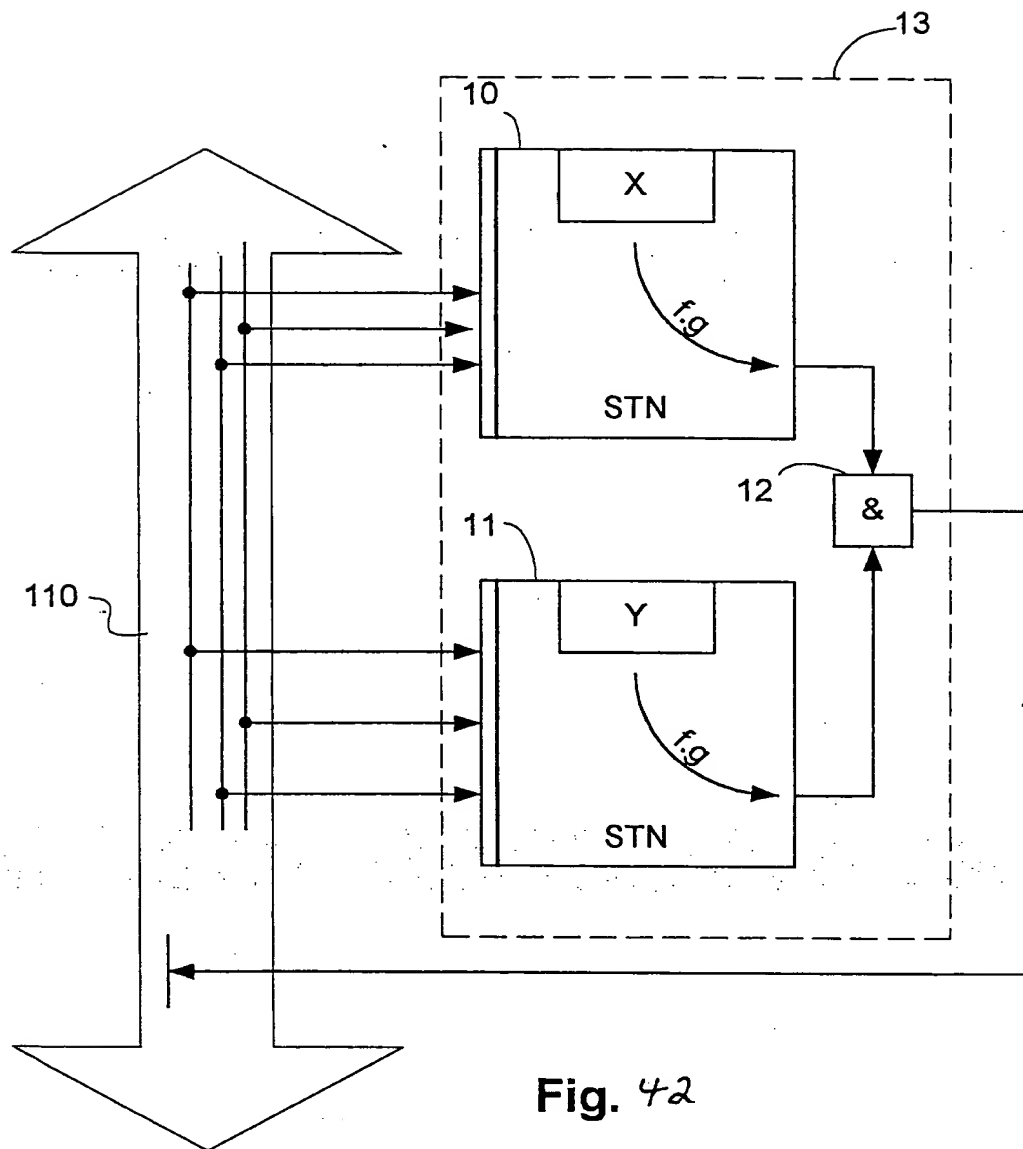


Fig. 41

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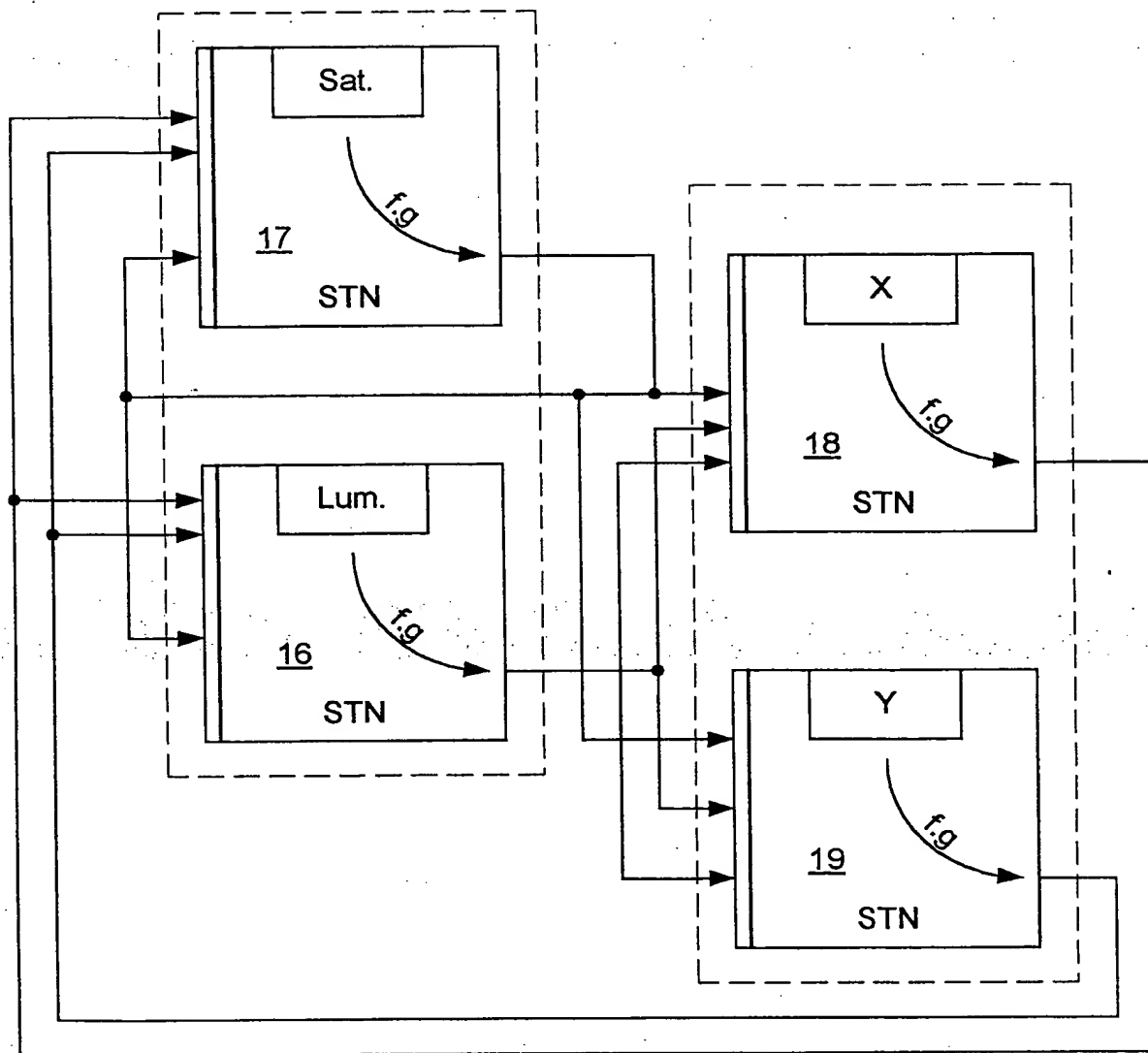


Fig. 44

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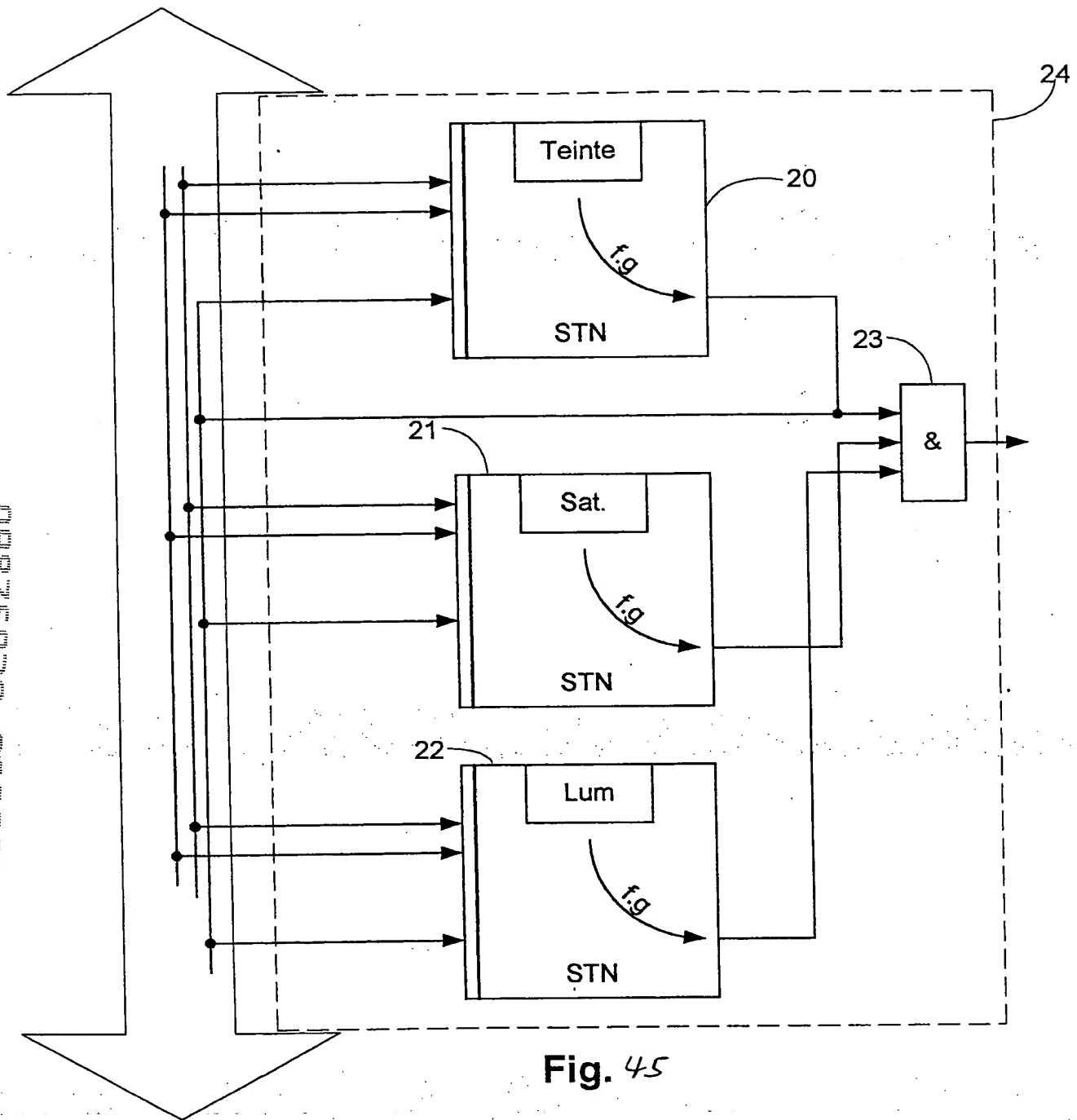


Fig. 45

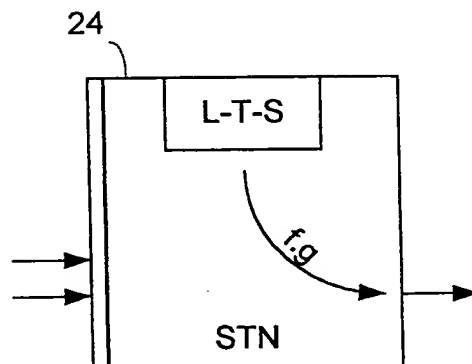


Fig. 46

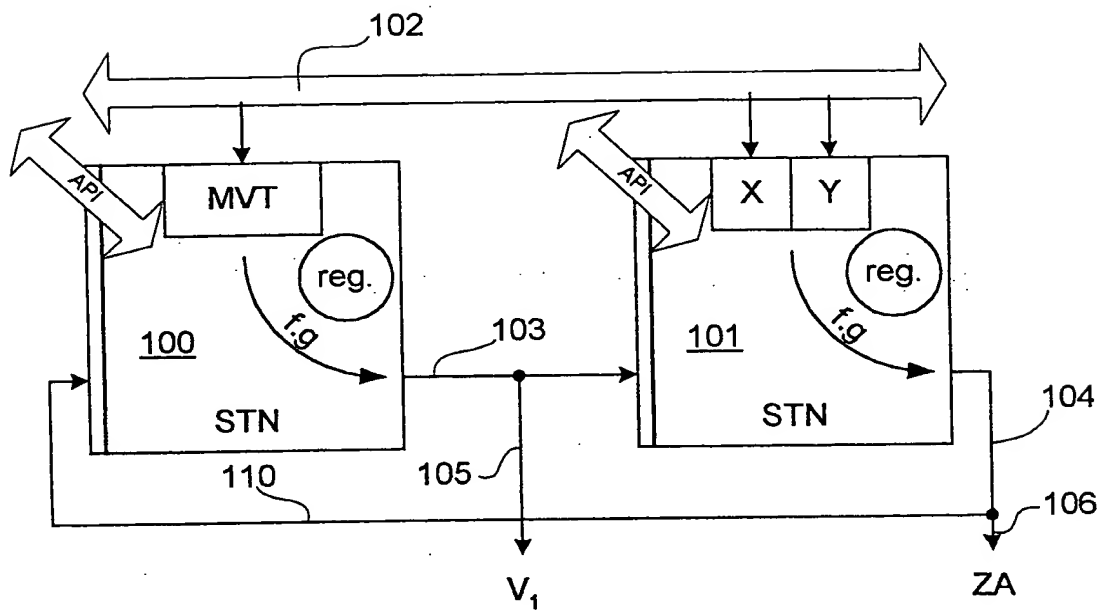


Fig. 47

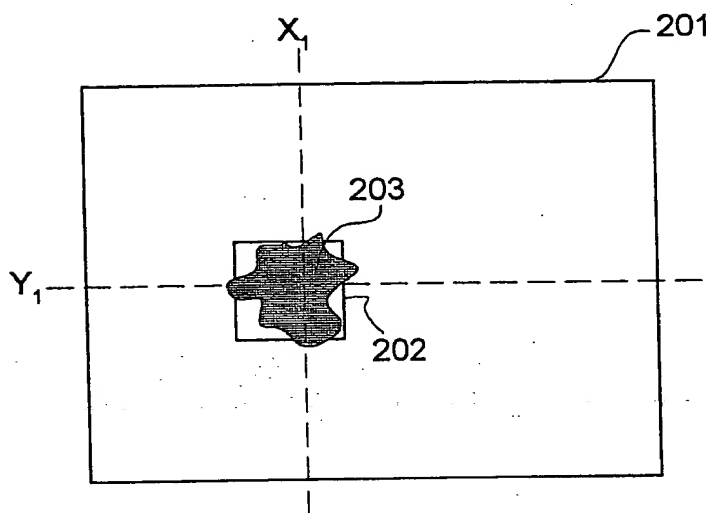


Fig. 48

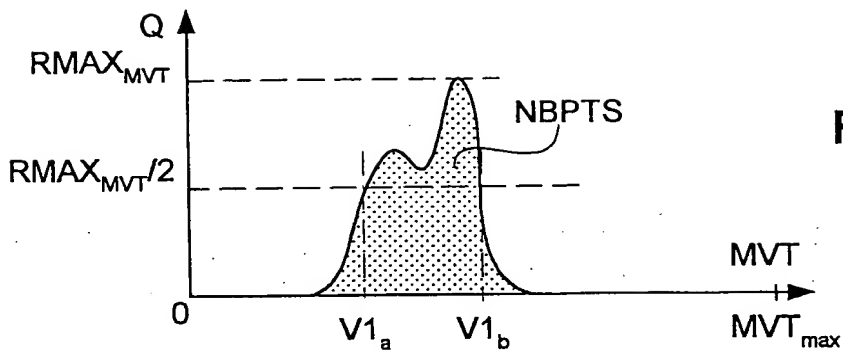


Fig. 49a

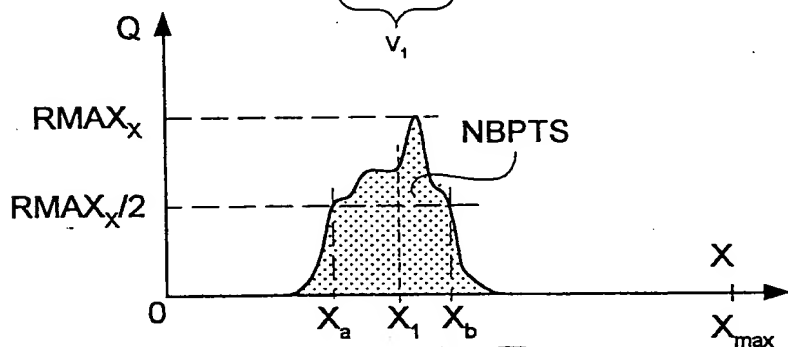


Fig. 49b

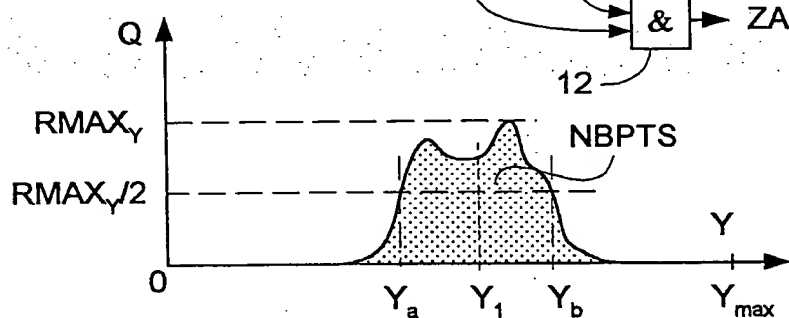


Fig. 49c

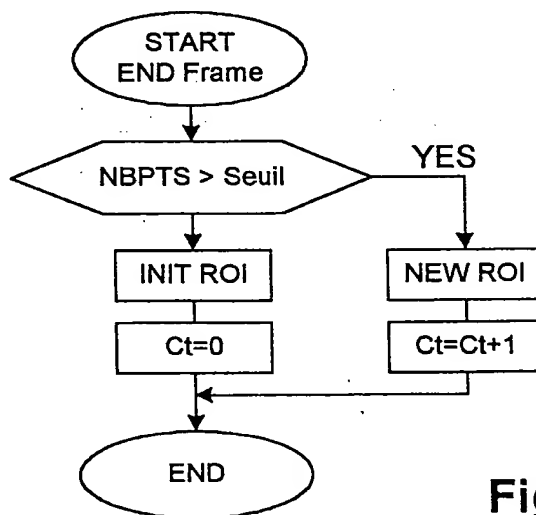


Fig. 50

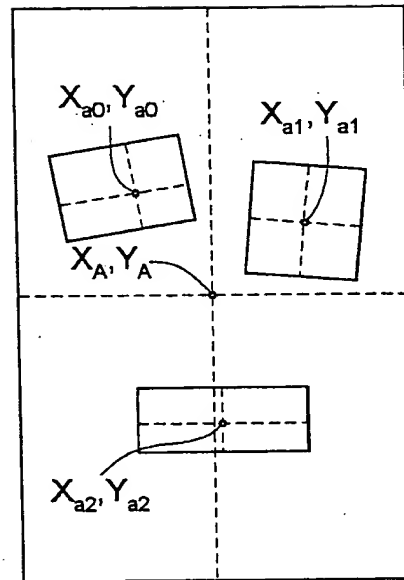
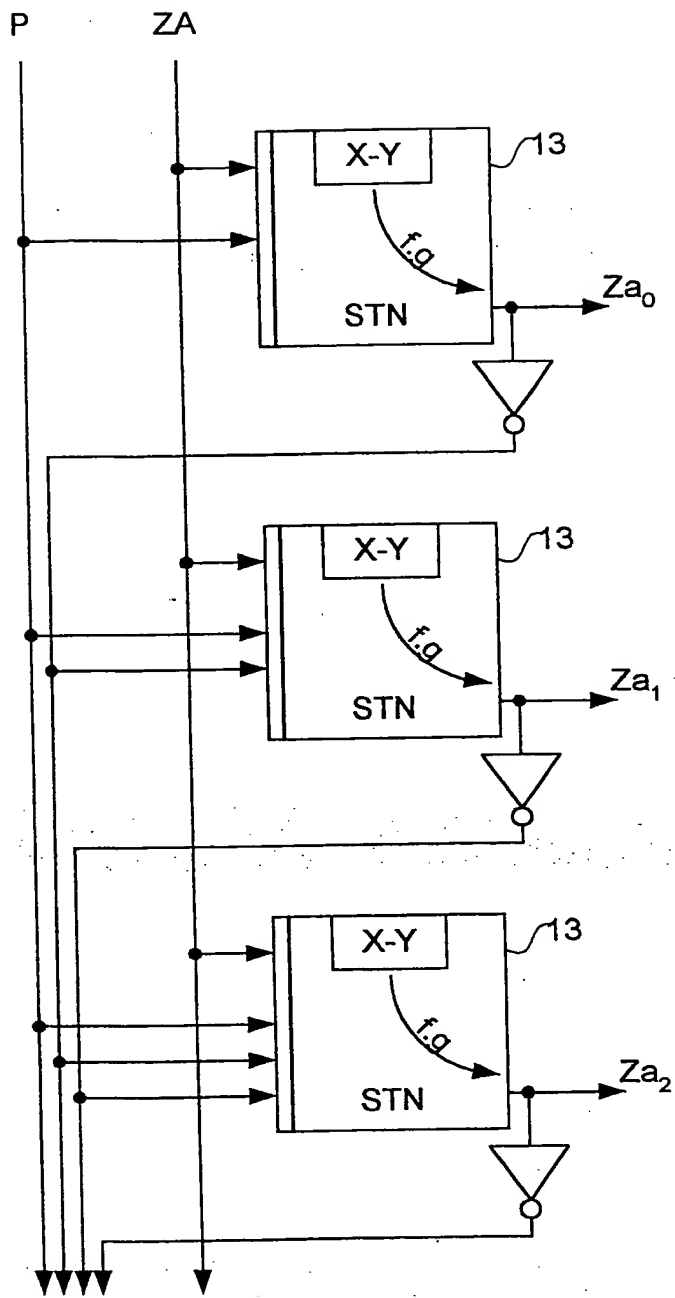


Fig. 54

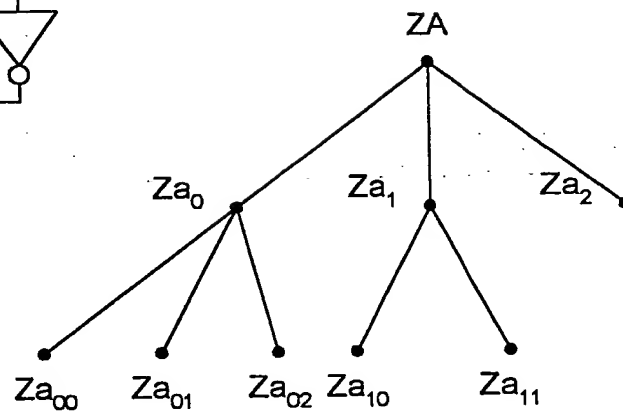


Fig. 52

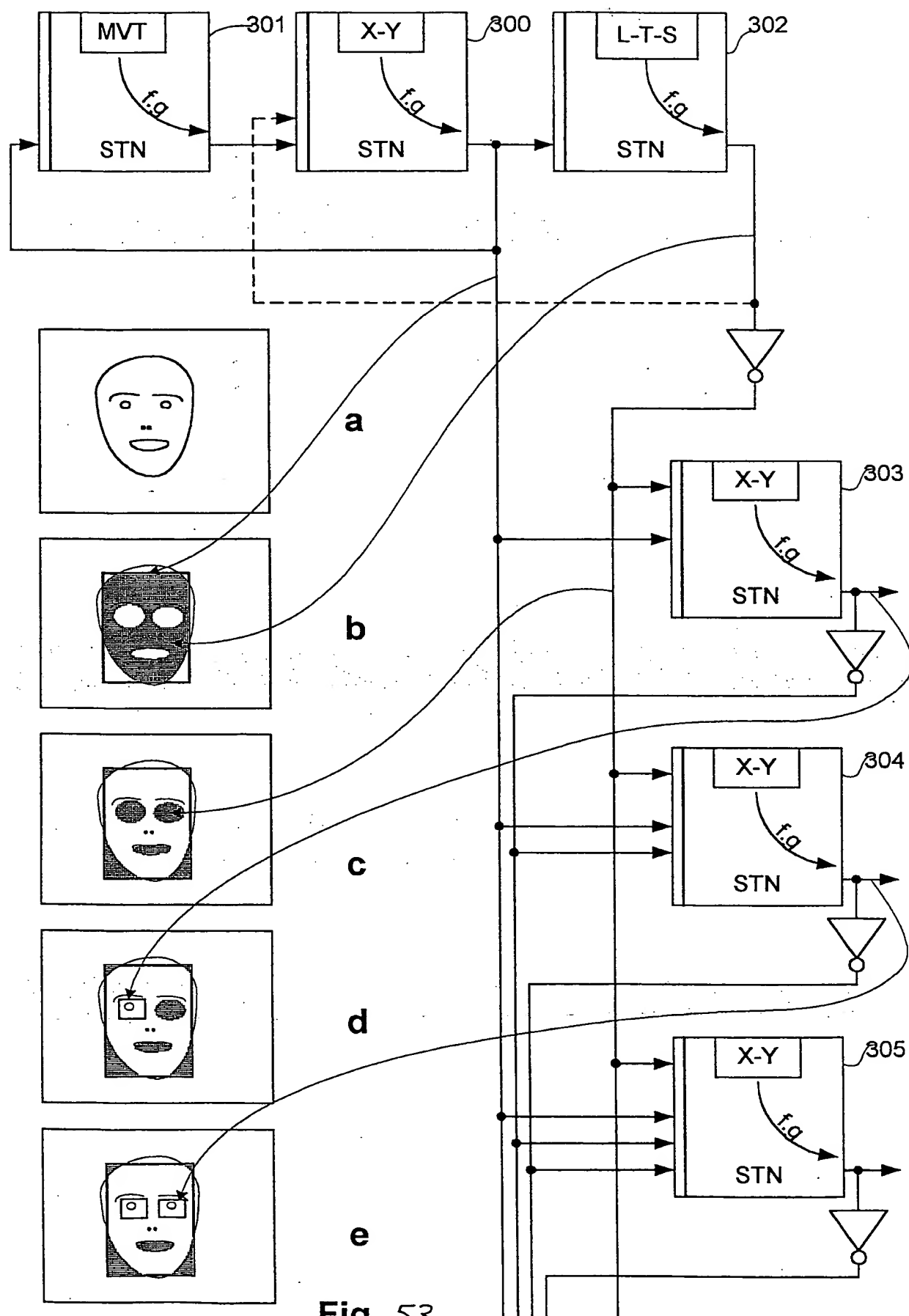


Fig. 53